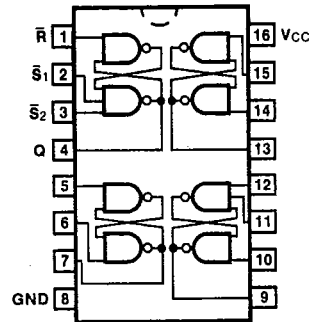


T-46-07-15

279

**54/74279**  
**54LS/74LS279**  
 QUAD SET-RESET LATCH

**CONNECTION DIAGRAM**  
 PINOUT A



4

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	74279PC, 74LS279PC		9B
Ceramic DIP (D)	A	74279DC, 74LS279DC	54279DM, 54LS279DM	6B
Flatpak (F)	A	74279FC, 74LS279FC	54279FM, 54LS279FM	4L

**TRUTH TABLE**

INPUTS			OUTPUT Q
S <sub>1</sub> -	S <sub>2</sub> -	R-	
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 h = The output is HIGH as long as S<sub>1</sub> or S<sub>2</sub> is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	20/10	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3\*

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I <sub>CC</sub>	Power Supply Current		30		7.0	mA	V <sub>CC</sub> = Max, R- = Gnd
t <sub>PLH</sub>	Propagation Delay S- to Q		22		22	ns	Figs. 3-1, 3-10
t <sub>PHL</sub>			15		15		
t <sub>PHL</sub>	Propagation Delay R- to Q		27		27	ns	Figs. 3-1, 3-10

\*DC limits apply over operating temperature range; AC limits apply at T<sub>A</sub> = +25°C and V<sub>CC</sub> = +5.0 V.