

SN74ALVC16820

3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS

SCAS268 – MARCH 1993 – REVISED MARCH 1994

- Member of the Texas Instruments *Widebus™* Family
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 10-bit flip-flop is designed specifically for low-voltage 3.3-V V_{CC} operation.

The flip-flops of the SN74ALVC16820 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16820 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16820 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE (TOP VIEW)

1OE	1	56	CLK
1Q1	2	55	D1
1Q2	3	54	NC
GND	4	53	GND
2Q1	5	52	D2
2Q2	6	51	NC
V _{CC}	7	50	V _{CC}
3Q1	8	49	D3
3Q2	9	48	NC
4Q1	10	47	D4
GND	11	46	GND
4Q2	12	45	NC
5Q1	13	44	D5
5Q2	14	43	NC
6Q1	15	42	D6
6Q2	16	41	NC
7Q1	17	40	D7
GND	18	39	GND
7Q2	19	38	NC
8Q1	20	37	D8
8Q2	21	36	NC
V _{CC}	22	35	V _{CC}
9Q1	23	34	D9
9Q2	24	33	NC
GND	25	32	GND
10Q1	26	31	D10
10Q2	27	30	NC
2OE	28	29	NC

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1994, Texas Instruments Incorporated

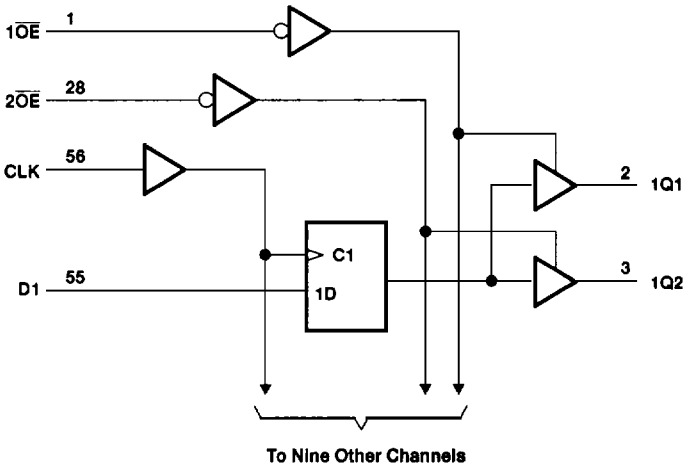
PRODUCT PREVIEW

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}_n^\dagger$	CLK	D	$Q_n^\dagger$
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	Q_0
H	X	X	Z

$^\dagger n = 1, 2$

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

SN74ALVC16820
3.3-V 10-BIT FLIP-FLOP
WITH DUAL OUTPUTS

SCAS268 – MARCH 1993 – REVISED MARCH 1994

recommended operating conditions

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V	-12		mA
		V _{CC} = 3 V	-24		
I _{OL}	Low-level output current	V _{CC} = 2.7 V	12		mA
		V _{CC} = 3 V	24		
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T _A	Operating free-air temperature		-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = −100 μA	MIN to MAX	V _{CC} −0.2		V	
	I _{OH} = −12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = −24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX	0.2		V	
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = V _{CC} or GND	3.6 V	±5		μA	
I _I (hold)	V _I = 0.8 V	3 V	75		μA	
	V _I = 2 V		−75			
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±10		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	40		μA	
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		750		μA	
C _i	V _I = V _{CC} or GND	3.3 V	4		pF	
C _o	V _O = V _{CC} or GND	3.3 V	6		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN74ALVC16820
3.3-V 10-BIT FLIP-FLOP
WITH DUAL OUTPUTS

SCAS268 – MARCH 1993 – REVISED MARCH 1994

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			VCC = 3.3 V ± 0.15 V		VCC = 3.3 V ± 0.3 V		VCC = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK high or low								ns
t _{su}	Setup time, data before CLK↑	High or low	0.8		1				ns
t _h	Hold time, data after CLK↑	High or low	2		2				ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 3.3 V ± 0.15 V		VCC = 3.3 V ± 0.3 V		VCC = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{max}			150		150		150		MHz
t _{PLH}	CLK	Q		4		4.5			ns
t _{PHL}				4		4.5			
t _{PZH}	OE	Q		5		5.7			ns
t _{PZL}				5		5.7			
t _{PHZ}	OE	Q		4.5		4.5			ns
t _{PLZ}				4.5		4.5			

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

