

# SN54BCT126A, SN74BCT126A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS252A – SEPTEMBER 1988 – REVISED APRIL 1994

- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (J, N)

## description

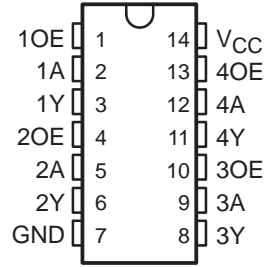
The 'BCT126A bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

The SN54BCT126A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74BCT126A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

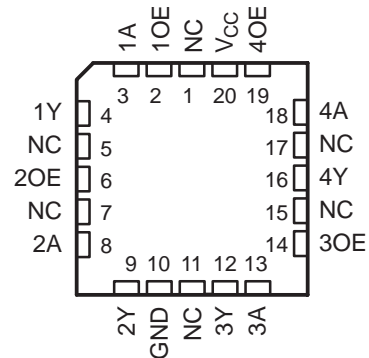
FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

SN54BCT126A . . . J OR W PACKAGE  
SN74BCT126A . . . D OR N PACKAGE  
(TOP VIEW)



SN54BCT126A . . . FK PACKAGE  
(TOP VIEW)

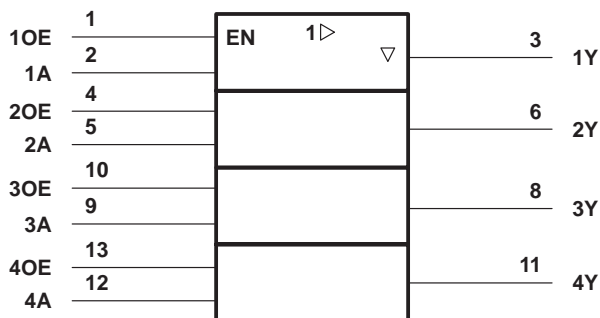


NC – No internal connection

# SN54BCT126A, SN74BCT126A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

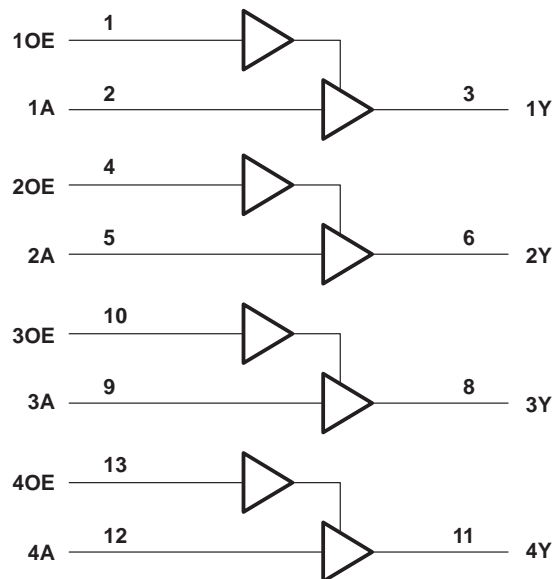
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



Pin numbers shown are for the J, N, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	– 0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	– 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ .....	– 0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$ .....	– 0.5 V to $V_{CC}$
Current into any output in the low state: SN54BCT126A .....	96 mA
SN74BCT126A .....	128 mA
Operating free-air temperature range: SN54BCT126A .....	– 55°C to 125°C
SN74BCT126A .....	0°C to 70°C
Storage temperature range .....	– 65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## recommended operating conditions

	SN54BCT126A			SN74BCT126A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$I_{IK}$ Input clamp current			–18			–18	mA
$I_{OH}$ High-level output current			–12			–15	mA
$I_{OL}$ Low-level output current			48			64	mA
$T_A$ Operating free-air temperature	–55		125	0		70	°C

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		SN54BCT126A			SN74BCT126A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5 V$ ,	$I_I = -18 mA$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 V$	$I_{OH} = -3 mA$	2.4	3.3		2.4	3.3		V
		$I_{OH} = -12 mA$	2	3.2					
		$I_{OH} = -15 mA$				2	3.1		
$V_{OL}$	$V_{CC} = 4.5 V$	$I_{OL} = 48 mA$		0.38	0.55				V
		$I_{OL} = 64 mA$					0.42	0.55	
$I_I$	$V_{CC} = 0$ ,	$V_I = 7 V$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5 V$ ,	$V_I = 2.7 V$			35			25	$\mu A$
$I_{IL}$	$V_{CC} = 5.5 V$ ,	$V_I = 0.5 V$			-20			-20	$\mu A$
$I_{OZH}$	$V_{CC} = 5.5 V$ ,	$V_O = 2.7 V$			50			50	$\mu A$
$I_{OZL}$	$V_{CC} = 5.5 V$ ,	$V_O = 0.5 V$			-50			-50	$\mu A$
$I_{OS}‡$	$V_{CC} = 5.5 V$ ,	$V_O = 0$	-100		-225	-100		-225	mA
$I_{CCH}$	$V_{CC} = 5.5 V$ ,	Outputs open		21	33		21	33	mA
$I_{CCL}$	$V_{CC} = 5.5 V$ ,	Outputs open		35	51		35	51	mA
$I_{CCZ}$	$V_{CC} = 5.5 V$ ,	Outputs open		5	10		5	10	mA
$C_i$	$V_{CC} = 5 V$ ,	$V_I = 2.5 V$ or $0.5 V$		4			4		pF
$C_o$	$V_{CC} = 5 V$ ,	$V_O = 2.5 V$ or $0.5 V$		9			9		pF

† All typical values are at  $V_{CC} = 5 V$ .

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

## switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V$ , $C_L = 50 pF$ , $R_1 = 500 \Omega$ , $R_2 = 500 \Omega$ , $T_A = 25^\circ C$			$V_{CC} = 4.5 V$ to $5.5 V$ , $C_L = 50 pF$ , $R_1 = 500 \Omega$ , $R_2 = 500 \Omega$ , $T_A = MIN$ to $MAX$ §				UNIT
			BCT126A			SN54BCT126A		SN74BCT126A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1.5	3.6	4.9	1.5	5.6	1.5	6.3	ns
$t_{PHL}$			2.7	5.3	6.9	2.7	7.7	2.7	7.4	
$t_{PZH}$	OE	Y	2.6	4.8	6.4	2.6	7.2	2.6	7.9	ns
$t_{PZL}$			3.7	6.4	8.3	3.7	10.5	3.7	10	
$t_{PHZ}$	OE	Y	3.2	6.6	8.2	3.2	9.6	3.2	10	ns
$t_{PLZ}$			3.4	6.5	8	3.4	12.3	3.4	10.7	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.





**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9088901M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9088901M2A SNJ54BCT 126AFK	<a href="#">Samples</a>
5962-9088901MCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9088901MC A SNJ54BCT126AJ	<a href="#">Samples</a>
5962-9088901MDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9088901MD A SNJ54BCT126AW	<a href="#">Samples</a>
SN54BCT126AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54BCT126AJ	<a href="#">Samples</a>
SNJ54BCT126AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9088901M2A SNJ54BCT 126AFK	<a href="#">Samples</a>
SNJ54BCT126AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9088901MC A SNJ54BCT126AJ	<a href="#">Samples</a>
SNJ54BCT126AW	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9088901MD A SNJ54BCT126AW	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14



J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

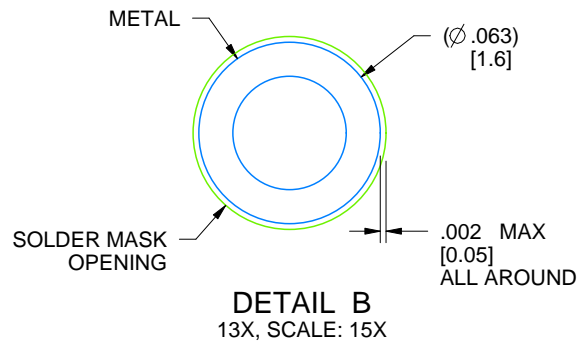
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



DETAIL A  
SCALE: 15X



DETAIL B  
13X, SCALE: 15X

4214771/A 05/2017

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