



**MOTOROLA**

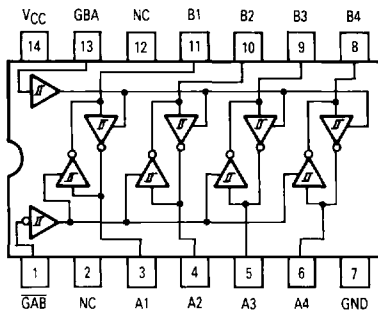
## Quad Bus Transceivers With 3-State Outputs

**ELECTRICALLY TESTED PER:  
MIL-M-38510/32801**

The 54LS242 is a Quad Bus Transmitter/Receiver designed for 4-line asynchronous 2-way data bus communications between data buses.

- Hysteresis at Inputs to Improve Noise Margins
- 2-Way Asynchronous Data Bus Communications
- Input Clamp Diodes Limit High-Speed Termination Effects

**LOGIC DIAGRAM**



**TRUTH TABLE**

Inputs		Output
$\overline{GAB}$	D	
L	L	H
L	H	L
H	X	(Z)

**TRUTH TABLE**

Inputs		Output
GBA	D	
L	X	(Z)
H	L	H
H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = HIGH Impedance

## Military 54LS242



**AVAILABLE AS:**

- 1) JAN: JM38510/32801BXA
- 2) SMD: 8002001
- 3) 883C: 54LS242/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: C  
CERFLAT: D  
LCC: 2

\*Call Factory for latest update

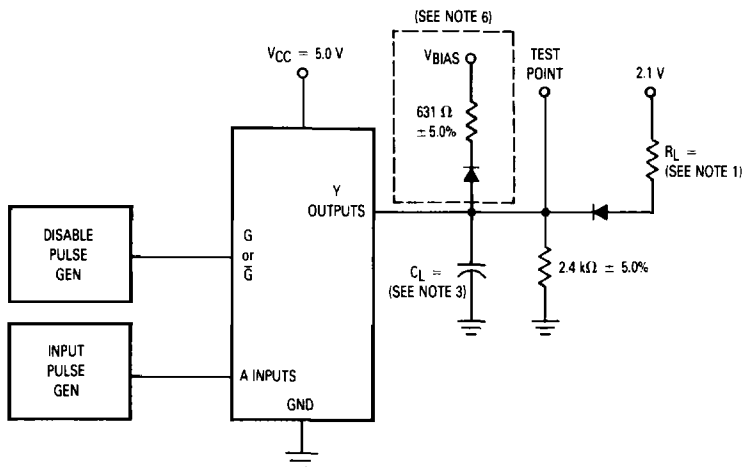
**PIN ASSIGNMENTS**

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{GAB}$	1	1	2	VCC
NC	2	2	3	VCC
A1	3	3	4	VCC
A2	4	4	6	VCC
A3	5	5	8	VCC
A4	6	6	9	VCC
GND	7	7	10	GND
B4	8	8	12	GND
B3	9	9	13	GND
B2	10	10	14	GND
B1	11	11	16	GND
NC	12	12	18	VCC
GBA	13	13	19	VCC
VCC	14	14	20	VCC

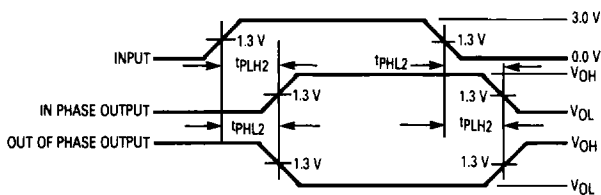
**BURN-IN CONDITIONS:**  
VCC = 5.0 V MIN/6.0 V MAX

# 54LS242

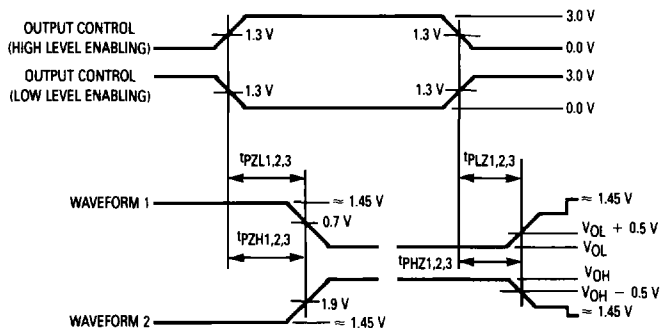
## AC TEST CIRCUIT



## WAVEFORMS



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times, Three-State Outputs

54LS242

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub> H	Logical "1" Output Voltage	2.4		2.4		2.4		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3.0 mA, V <sub>IN</sub> = 2.0 V (all inputs), $\overline{\text{GAB}}/\text{GBA} = 0.7 \text{ V}$ or 2.0 V per truth table.
V <sub>OH</sub> L	Logical "1" Output Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA, V <sub>IN</sub> = 0.5 V (all inputs), $\overline{\text{GAB}}/\text{GBA} = 2.0 \text{ V}$ or 0.5 V per truth table.
V <sub>OL</sub>	Logical "0" Output Voltage		0.4		0.4		0.4	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA, V <sub>IN</sub> = 2.0 V (all inputs), $\overline{\text{GAB}}/\text{GBA} = 2.0 \text{ V}$ or 0.7 V per truth table.
V <sub>IC</sub>	Input Clamping Voltage		-1.5					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open, $\overline{\text{GAB}}/\text{GBA} = \text{GND}$ , open, 5.5 V, 4.5 V per truth table.
I <sub>IH</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs are open, $\overline{\text{GAB}}/\text{GBA} = 5.5 \text{ V}$ , 2.7 V or GND per truth table.
I <sub>IHH</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, other inputs are open, $\overline{\text{GAB}}/\text{GBA} = 0 \text{ V}$ , 4.5 V, 5.5 V or open per truth table.
I <sub>IL</sub>	Logical "0" Input Current	0	-150	0	-150	0	-150	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V, other inputs are open, $\overline{\text{GAB}}/\text{GBA} = \text{GND}$ , 0.4 V, 4.5 V, 5.5 V per truth table.
I <sub>OS</sub>	Output Short Circuit Current	-40	-225	-40	-225	-40	-225	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = GND, other inputs are open, $\overline{\text{GAB}}/\text{GBA} = \text{GND}$ or 4.5 V per truth table.
I <sub>IOZH</sub>	Output Off Current High		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V, other inputs are open, $\overline{\text{GAB}} = 2.0 \text{ V}$ or open, $\text{GBA} = 0.7 \text{ V}$ or open.
I <sub>IOZL</sub>	Output Off Current Low		-200		-200		-200	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V, other inputs are open, $\overline{\text{GAB}} = 2.0 \text{ V}$ or open, $\text{GBA} = 0.7 \text{ V}$ or open.
I <sub>CC</sub> H	Power Supply Current		38		38		38	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = GND (all inputs), $\overline{\text{GAB}}/\text{GBA} = \text{GND}$ .
I <sub>CC</sub> L	Power Supply Current		50		50		50	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (all inputs), $\overline{\text{GAB}}/\text{GBA} = \text{GND}$ .
I <sub>CC</sub> Z	Power Supply Current Off		50		50		50	mA	V <sub>CC</sub> = 5.5 V, all inputs are open, $\overline{\text{GAB}} = 5.5 \text{ V}$ , $\text{GBA} = \text{GND}$ .
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.7		0.7		0.7	V	V <sub>CC</sub> = 4.5 V.
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V <sub>CC</sub> = 5.0 V, V <sub>INL</sub> = 0.4 V, and V <sub>INH</sub> = 2.4 V.

## 54LS242

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
tPHL2 tPHL2	Propagation Delay /Data-Output Output <u>High-Low</u>	2.0	23 18	2.0	30 25	2.0	30 25	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 110 Ω. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.
tPLH2 tPLH2	Propagation Delay /Data-Output Output <u>Low-High</u>	2.0	19 14	2.0	25 20	2.0	25 20	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 110 Ω. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.
tPLZ1 tPLZ1	Propagation Delay /Data-Output Output <u>Low-High</u>	2.0	30 25	2.0	39 34	2.0	39 34	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 110 Ω. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.
tPHZ1 tPHZ1	Propagation Delay /Data-Output Output <u>High-Low</u>	2.0	35 18	2.0	46 41	2.0	46 41	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 110 Ω. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.
tPZL1 tPZL1	Propagation Delay /Data-Output Output <u>Low-High</u>	2.0	35 30	2.0	46 41	2.0	46 41	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 110 Ω. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.
tPZH1 tPZH1	Propagation Delay /Data-Output Output <u>High-Low</u>	2.0	28 23	2.0	36 31	2.0	36 31	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 110 Ω. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω.

**NOTES:**

1. R<sub>L</sub> = 110 Ω ± 5.0%
2. All diodes are 1N3064 or equivalent.
3. C<sub>L</sub> = 50 pF ± 10% including probe and jig capacitance.
4. The pulse generators have the following characteristics:  
V<sub>gen</sub> = 3.0 V, PRR ≤ 1.0 MHz, t<sub>r</sub> ≤ 15 ns, t<sub>f</sub> = 6.0 ns, Z<sub>OUT</sub> = 50 Ω.
5. Clock pulse characteristics: t<sub>p(clock)</sub> = 20 ns, t<sub>setup</sub> = 20 ns.
6. The diode and resistor shown within the dotted area are optional. When the diode and resistor are used, V<sub>BIAS</sub> shall be 5.5 V for all tests except for tPHZ, for tPHZ tests, V<sub>BIAS</sub> shall be -0.6 V.