EL5172

250MHz Differential Line Receiver

FN7311
Rev.12.00
Jul 30, 2020

The EL5172 is a single high bandwidth amplifier designed to extract the difference signal from noisy environments. It is primarily targeted for applications such as receiving signals from twisted-pair lines or any application where common mode noise injection is likely to occur.

The EL5172 is stable for a gain of one and requires two external resistors to set the voltage gain.

The output common mode level is set by the reference pin (V_{REF}), which has a -3dB bandwidth of over 120MHz. Generally, this pin is grounded but it can be tied to any voltage reference.

The output can deliver a maximum of ±60mA and is short-circuit protected to withstand a temporary overload condition.

The EL5172 is available in the 8 Ld SOIC and 8 Ld MSOP packages. It is specified for operation across the full -40°C to +85°C temperature range.

Related Literature

For a full list of related documents, visit our website:

- EL5172 device page

Features

- Differential input range ±2.3V
- 250MHz 3dB bandwidth
- 800V/µs slew rate
- 60mA maximum output current
- Single 5V or dual ±5V supplies
- Low power - 5mA to 6mA
- Pb-free available (RoHS compliant)

Applications

- Twisted-pair receivers
- Differential line receivers
- VGA over twisted-pair
- ADSL/HDSL receivers
- Differential to single-ended amplification
- Reception of analog signals in a noisy environment

Ordering Information

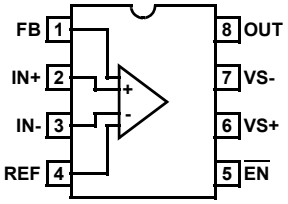
PART NUMBER	PART MARKING	TAPE AND REEL (Units)	PACKAGE (RoHS Compliant)	PKG. DWG. #
EL5172ISZ	5172ISZ	-	8 Ld SOIC (150 mil)	M8.15E
EL5172ISZ-T7	5172ISZ	1k	8 Ld SOIC (150 mil)	M8.15E
EL5172ISZ-T7A	5172ISZ	250	8 Ld SOIC (150 mil)	M8.15E
EL5172ISZ-T13	5172ISZ	2.5k	8 Ld SOIC (150 mil)	M8.15E
EL5172IYZ	BAAWA	-	8 Ld MSOP (3.0mm)	M8.118A
EL5172IYZ-T7	BAAWA	1.5k	8 Ld MSOP (3.0mm)	M8.118A
EL5172IYZ-T13	BAAWA	2.5k	8 Ld MSOP (3.0mm)	M8.118A

NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the EL5172 device page. For more information about MSL, see TB363.

Pinout

(8 LD SOIC, MSOP)
TOP VIEW



Pin Descriptions

PIN NUMBERS	PIN NAME	PIN FUNCTION
1	FB	Feedback input
2	IN+	Non-inverting input
3	IN-	Inverting input
4	REF	Sets the common mode output voltage level
5	$\overline{EN}$	Enabled when this pin is floating or the applied voltage $\leq V_S+ - 1.5$
6	VS+	Positive supply voltage
7	VS-	Negative supply voltage
8	OUT	Output voltage

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_S+ to V_S-) 12V
Supply Voltage Rate-of-rise (dV/dT) 1V/µs
Input Voltage (IN+, IN- to V_S+, V_S-). . . . . V_S- - 0.3V to V_S+ + 0.3V
Differential Input Voltage (IN+ to IN-). . . . . ±4.8V
Maximum Output Current. . . . . ±60mA

Thermal Information

Operating Junction Temperature . . . . . .+135°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Storage Temperature Range . . . . . .-65°C to +150°C
Power Dissipation . . . . . See Curves
Pb-free reflow profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, T_A = +25°C, V_{IN} = 0V, R_L = 500Ω, R_F = 0, R_G = OPEN, C_L = 2.7pF, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	A_V =1, C_L = 2.7pF		250		MHz
		A_V =2, R_F = 1000Ω, C_L = 2.7pF		70		MHz
		A_V =10, R_F = 1000Ω, C_L = 2.7pF		10		MHz
BW	±0.1dB Bandwidth	A_V =1, C_L = 2.7pF		25		MHz
SR	Slew Rate	V_{OUT} = 3V_{P-P}, 20% to 80%	550	800	1000	V/µs
t_{STL}	Settling Time to 0.1%	V_{OUT} = 2V_{P-P}		10		ns
t_{OVR}	Output Overdrive Recovery Time			20		ns
GBWP	Gain Bandwidth Product			100		MHz
V_{REF}BW (-3dB)	V_{REF} -3dB Bandwidth	A_V =1, C_L = 2.7pF		120		MHz
V_{REF}SR	V_{REF} Slew Rate	V_{OUT} = 2V_{P-P}, 20% to 80%		600		V/µs
V_N	Input Voltage Noise	at f = 11kHz		26		nV/√Hz
I_N	Input Current Noise	at f = 11kHz		2		pA/√Hz
HD2	Second Harmonic Distortion	V_{OUT} = 1V_{P-P}, 5MHz		-66		dBc
		V_{OUT} = 2V_{P-P}, 50MHz		-63		dBc
HD3	Third Harmonic Distortion	V_{OUT} = 1V_{P-P}, 5MHz		-84		dBc
		V_{OUT} = 2V_{P-P}, 50MHz		-76		dBc
dG	Differential Gain at 3.58MHz	R_L = 150Ω, A_V = 2		0.04		%
dθ	Differential Phase at 3.58MHz	R_L = 150Ω, A_V = 2		0.41		°
INPUT CHARACTERISTICS						
V_{OS}	Input Referred Offset Voltage			±7	±25	mV
I_{IN}	Input Bias Current (V_{IN}, V_{INB}, V_{REF})		-14	-6	-3	µA
R_{IN}	Differential Input Resistance			300		kΩ
C_{IN}	Differential Input Capacitance			1		pF
DMIR	Differential Input Range		±2.1	±2.38	±2.5	V
CMIR+	Common Mode Positive Input Range at V_{IN}+, V_{IN}-		3.3	3.5		V
CMIR-	Common Mode Positive Input Range at V_{IN}+, V_{IN}-			-4.5	-4.3	
V_{REFIN+}	Reference Input Positive Voltage Range	V_{IN}+ = V_{IN}- = 0V	3.3	3.7		V
V_{REFIN-}	Reference Input Negative Voltage Range	V_{IN}+ = V_{IN}- = 0V		-3.9	-3.6	
CMRR	Input Common Mode Rejection Ratio	V_{IN} = ±2.5V	75	95		dB
Gain	Gain Accuracy	V_{IN} = 1	0.985	1	1.015	V

Electrical Specifications $V_S+ = +5V$, $V_S- = -5V$, $T_A = +25°C$, $V_{IN} = 0V$, $R_L = 500\Omega$, $R_F = 0$, R_G = OPEN, $C_L = 2.7pF$, Unless Otherwise Specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS						
V_{OUT}	Positive Output Voltage Swing	$R_L = 500\Omega$ to GND	3.3	3.63		V
	Negative Output Voltage Swing	$R_L = 500\Omega$ to GND		-3.87	-3.5	V
I_{OUT}(Max)	Maximum Output Current	$R_L = 10\Omega$	±60	±95		mA
R_{OUT}	Output Impedance			100		mΩ
SUPPLY						
V_{SUPPLY}	Supply Operating Range	V_S+ to V_S-	4.75		11	V
$I_{S\ (on)}$	Power Supply Current - Enabled		4.6	5.6	7	mA
$I_{S\ (off)}+$	Positive Power Supply Current - Disabled	$\overline{EN}$ pin tied to 4.8V		80	100	µA
$I_{S\ (off)}-$	Negative Power Supply Current - Disabled		-150	-120	-90	µA
PSRR	Power Supply Rejection Ratio	V_S from ±4.5V to ±5.5V	50	58		dB
ENABLE						
t_{EN}	Enable Time			150		ns
t_{DS}	Disable Time			1.4		µs
V_{IH}	$\overline{EN}$ Pin Voltage for Power-up				$V_S+ - 1.5$	V
V_{IL}	$\overline{EN}$ Pin Voltage for Shutdown		$V_S+ - 0.5$			V
I_{IH-EN}	$\overline{EN}$ Pin Input Current High	At $V_{EN} = 5V$		40	60	µA
I_{IL-EN}	$\overline{EN}$ Pin Input Current Low	At $V_{EN} = 0V$	-10	-3		µA

Typical Performance Curves

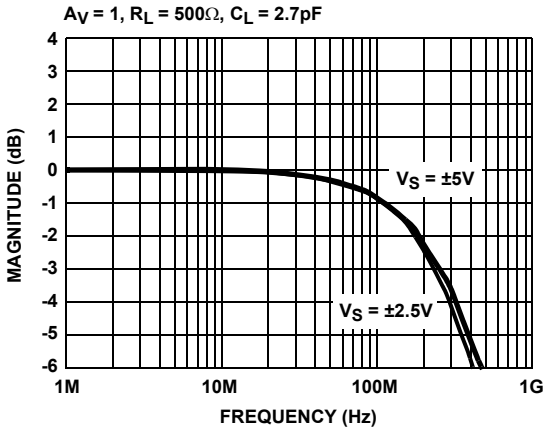


FIGURE 1. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

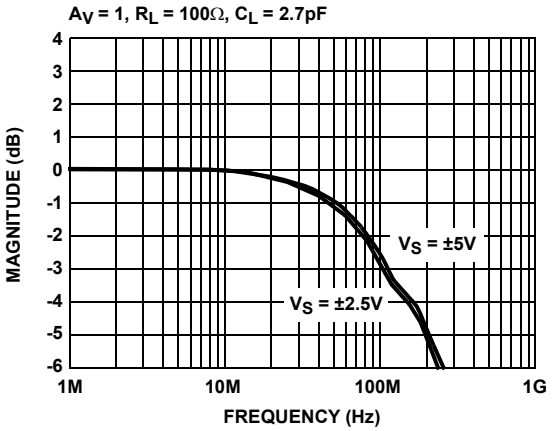


FIGURE 2. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

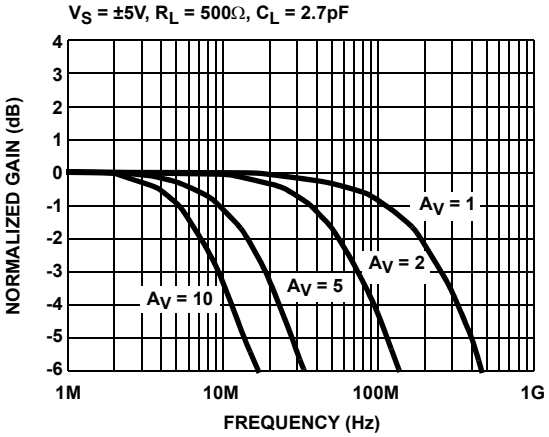


FIGURE 3. FREQUENCY RESPONSE vs VARIOUS GAIN

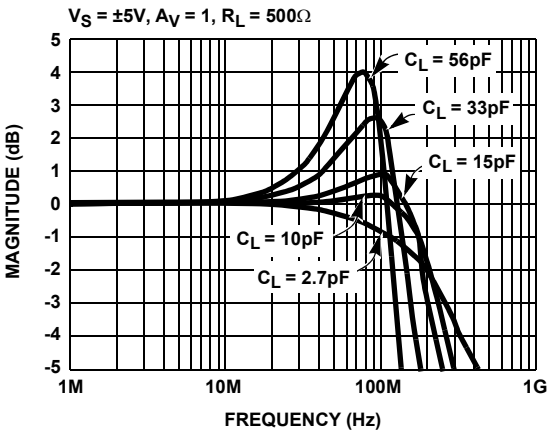


FIGURE 4. FREQUENCY RESPONSE vs C_L

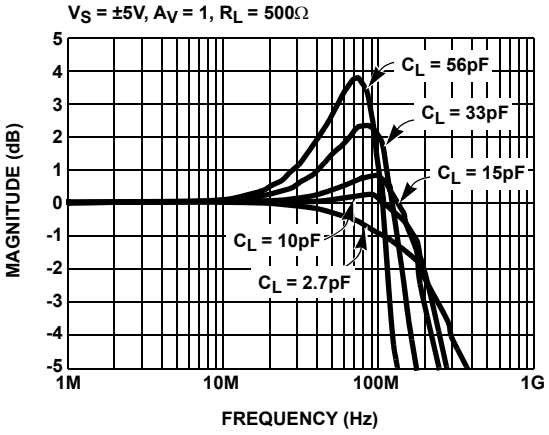


FIGURE 5. FREQUENCY RESPONSE vs C_L

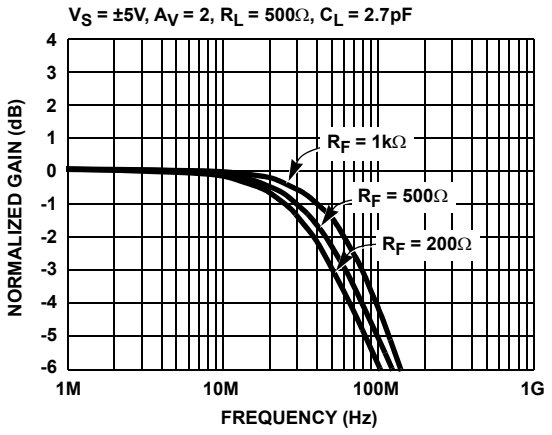


FIGURE 6. FREQUENCY RESPONSE FOR VARIOUS R_F

Typical Performance Curves (Continued)

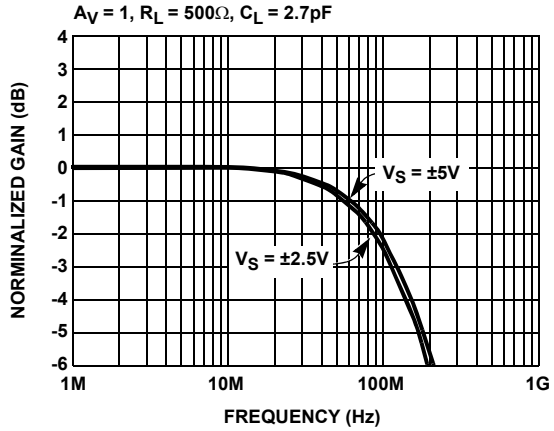


FIGURE 7. FREQUENCY RESPONSE FOR V_{REF}

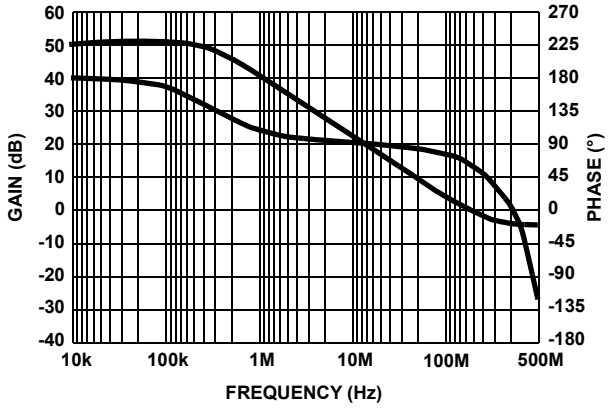


FIGURE 8. OPEN LOOP GAIN

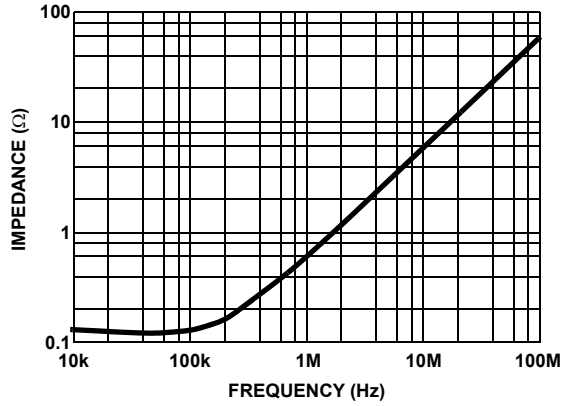


FIGURE 9. OUTPUT IMPEDANCE vs FREQUENCY

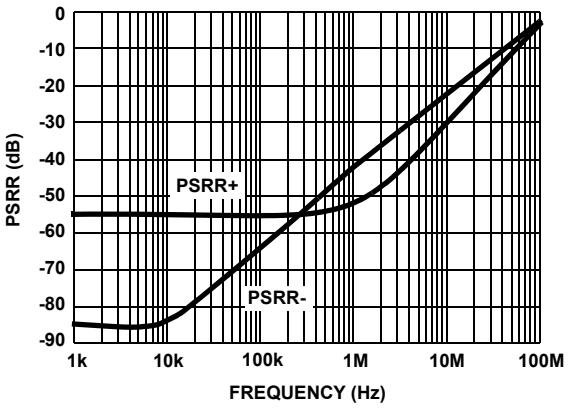


FIGURE 10. PSRR vs FREQUENCY

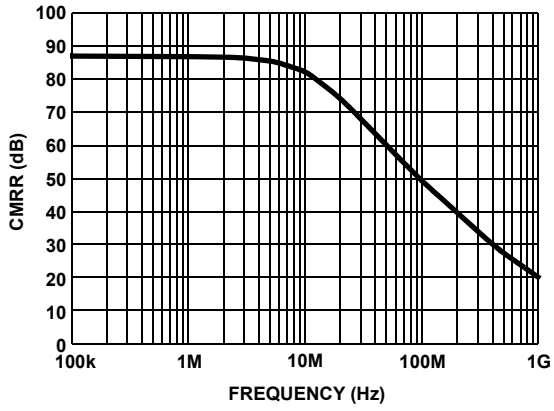


FIGURE 11. CMRR vs FREQUENCY

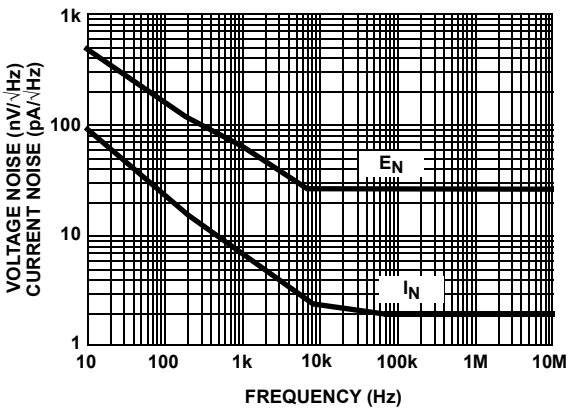


FIGURE 12. VOLTAGE AND CURRENT NOISE vs FREQUENCY

Typical Performance Curves (Continued)

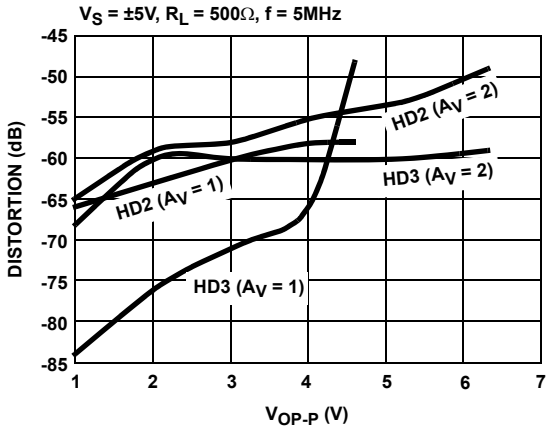


FIGURE 13. HARMONIC DISTORTION vs OUTPUT VOLTAGE

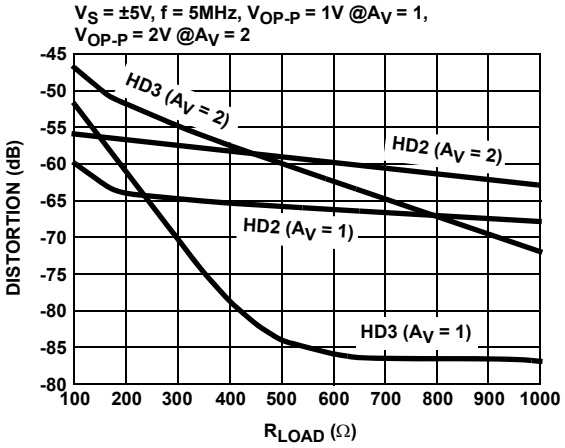


FIGURE 14. HARMONIC DISTORTION vs LOAD RESISTANCE

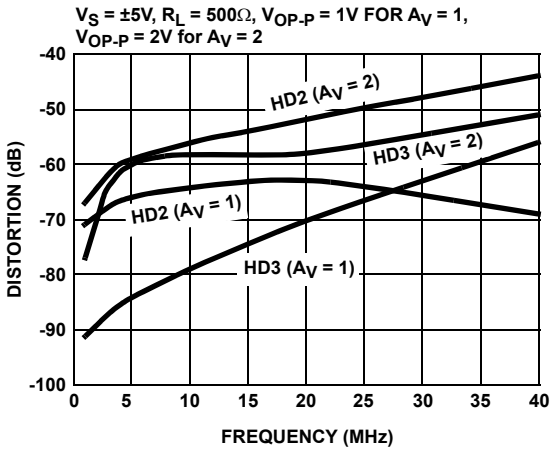


FIGURE 15. HARMONIC DISTORTION vs FREQUENCY

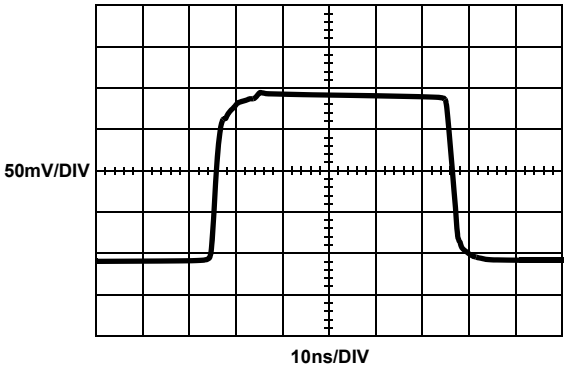


FIGURE 16. SMALL SIGNAL TRANSIENT RESPONSE

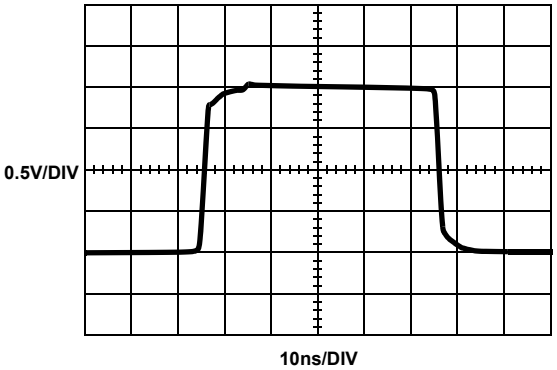


FIGURE 17. LARGE SIGNAL TRANSIENT RESPONSE

Typical Performance Curves (Continued)

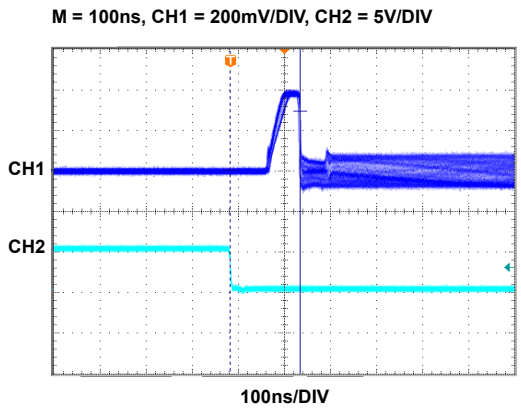


FIGURE 18. ENABLED RESPONSE

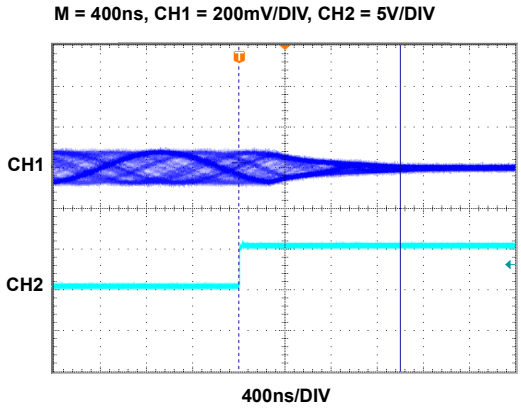


FIGURE 19. DISABLED RESPONSE

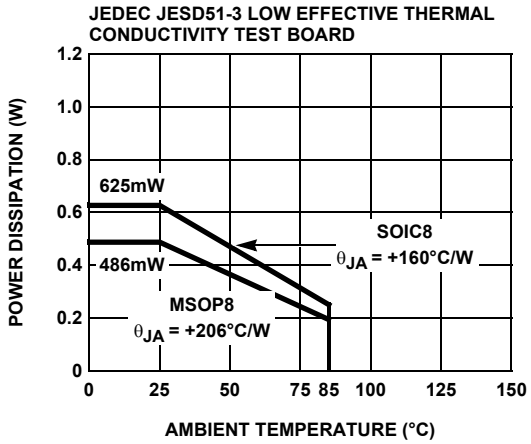


FIGURE 20. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

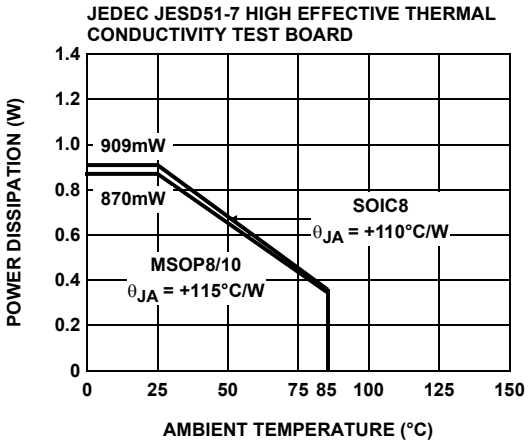
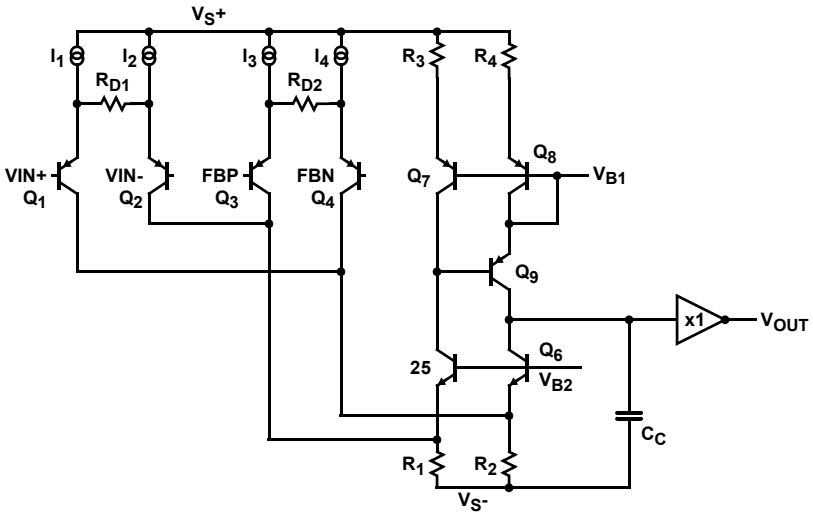


FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Simplified Schematic



Description of Operation and Application Information

Product Description

The EL5172 is a low-power, wideband, differential to single-ended amplifier. The EL5172 is internally compensated for closed loop gain of +1 or greater. Connected in gain of 1 and driving a 500Ω load, the EL5172 has a -3dB bandwidth of 250MHz. Driving a 150Ω load at gain of 2, the bandwidth is about 50MHz. The bandwidth at the REF input is about 450MHz. The EL5172 is available with a power-down feature to reduce the power while the amplifier is disabled.

Input, Output and Supply Voltage Range

The EL5172 is designed to operate with a single supply voltage of 5V to 10V or split supplies with its total voltage from 5V to 10V. The amplifier has an input common mode voltage range from -4.3V to 3.3V for ±5V supply. The differential mode input range (DMIR) between the two inputs is about from -2.3V to +2.3V. The input voltage range at the REF pin is from -3.6V to 3.3V. If the input common mode or differential mode signal is outside the above-specified ranges, it will cause the output signal to be distorted.

The output of the EL5172 can swing from -3.8V to 3.6V at 500Ω load at ±5V supply. As the load resistance becomes lower, the output swing is reduced respectively.

Overall Gain Settings

The gain setting for the EL5172 is similar to the conventional operational amplifier. The output voltage is equal to the difference of the inputs plus V_{REF} and then times the gain, as expressed in Equation 1.

$$V_O = (V_{IN}+ - V_{IN}- + V_{REF}) \times \left(1 + \frac{R_F}{R_G}\right) \quad \text{(EQ. 1)}$$

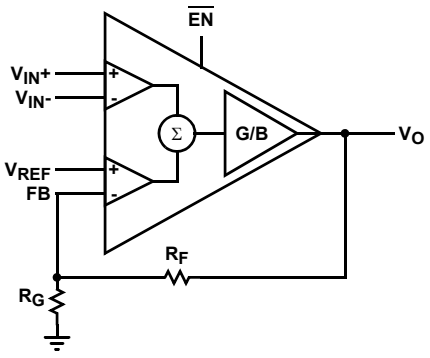


FIGURE 22.

Choice of Feedback Resistor and Gain Bandwidth Product

For applications that require a gain of +1, no feedback resistor is required; just short the OUT pin to the FB pin. For gains greater than +1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes smaller, the amplifier's phase margin is reduced. This causes ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value that should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few Pico farad range in parallel with R_F can help to reduce the ringing and peaking at the expense of reducing the bandwidth.

The bandwidth of the EL5172 depends on the load and the feedback network. R_F and R_G appear in parallel with the load for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F also has a minimum value that should not be exceeded for optimum bandwidth performance. For a gain of +1, $R_F = 0$ is optimum. For the gains other than +1, optimum response is obtained with R_F between 500Ω to 1kΩ. For $A_V = 2$ and $R_F = R_G =$ 1kΩ, the BW is about 80MHz and the frequency response is very flat.

The EL5172 has a gain bandwidth product of 100MHz. For gains ≥5, its bandwidth can be predicted using Equation 2:

$$\text{Gain} \times \text{BW} = 100\text{MHz} \quad \text{(EQ. 2)}$$

Driving Capacitive Loads and Cables

The EL5172 can drive 56pF capacitance in parallel with 500Ω load to ground with 4dB of peaking at a gain of +1. If less peaking is desired in applications, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with each output to eliminate most peaking. However, this will reduce the gain slightly. If the gain setting is greater than 1, the gain resistor R_G can then be chosen to make-up for any gain loss which may be created by the additional series resistor at the output.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down

The EL5172 can be disabled and its outputs placed in a high impedance state. The turn-off time is about 1.4µs and the turn-on time is about 150ns. When disabled, the amplifier's supply current is reduced to 80µA for I_S+ and 120µA for I_S- typically, thereby effectively eliminating the power consumption. The amplifier's power-down can be controlled by standard CMOS signal levels at the ENABLE pin. The applied logic signal is relative to V_S+ pin. Letting the $\overline{EN}$ pin float or applying a signal that is less than 1.5V below V_S+ enables the amplifier. The amplifier will be disabled when the signal at $\overline{EN}$ pin is above V_S+ - 0.5V. If a TTL signal controls

the enabled/disabled function, Figure 23 could be used to convert the TTL signal to CMOS signal.

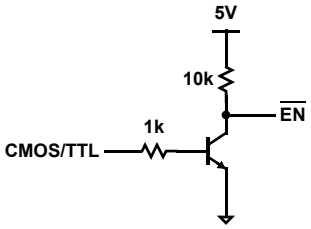


FIGURE 23.

Output Drive Capability

The EL5172 has internal short-circuit protection. Its typical short-circuit current is ±95mA. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±60mA. This limit is set by the design of the internal metal interconnections.

Power Dissipation

With the high output drive capability of the EL5172, it is possible to exceed the +135°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 3:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 3)}$$

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package

Assuming the REF pin is tied to GND for V_S = ±5V application, the maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

For sourcing, use Equation 4:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S + - V_{OUT}) \times \frac{V_{OUT}}{R_{LOAD}} \quad \text{(EQ. 4)}$$

For sinking, use Equation 5:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_{OUT} - V_S-) \times I_{LOAD} \quad \text{(EQ. 5)}$$

Where:

- V_S = Total supply voltage
- I_{SMAX} = Maximum quiescent supply current
- V_{OUT} = Maximum output voltage of the application
- R_{LOAD} = Load resistance
- I_{LOAD} = Load current

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LOAD} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_S- pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to a minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

Typical Applications

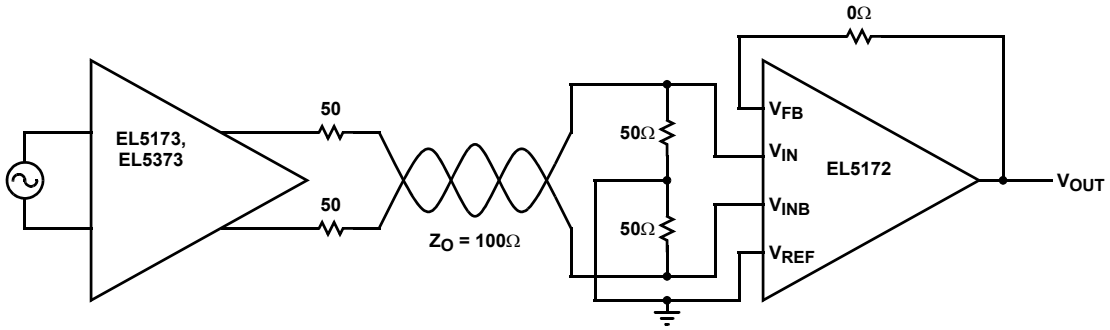


FIGURE 24. TWISTED PAIR CABLE RECEIVER

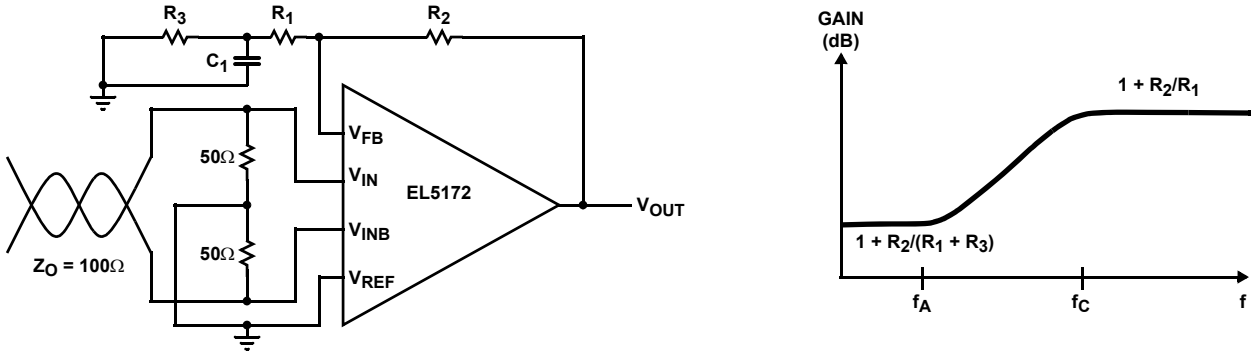


FIGURE 25. COMPENSATED LINE RECEIVER

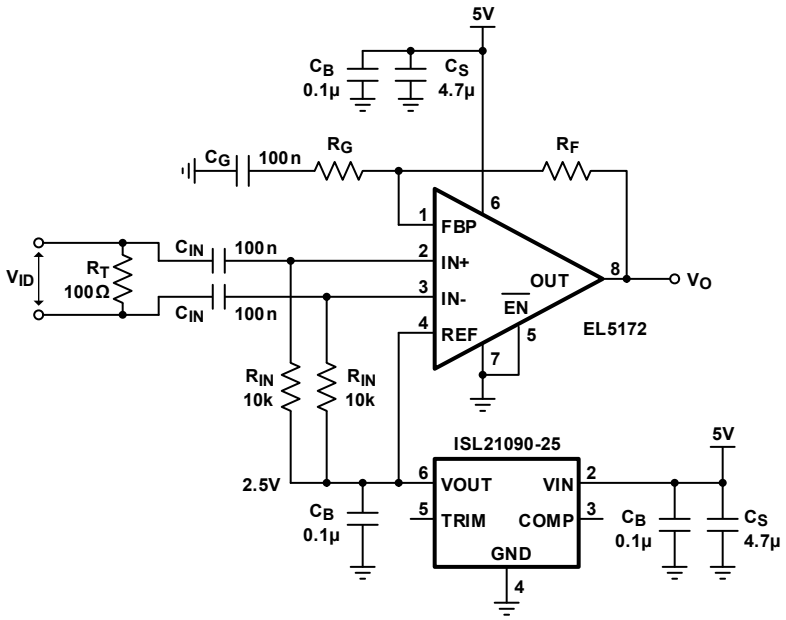


FIGURE 26. Single Supply Operation

As the signal is transmitted through a cable, the high frequency signal will be attenuated. One way to compensate for this loss is to boost the high frequency gain at the receiver side.

Level Shifter and Signal Summer

The EL5172 contains two pairs of differential pair input stages, which make sure that the inputs are all high impedance inputs. To take advantage of the two high impedance inputs, the EL5172 can be used as a signal summer to add two signals together. One signal can be applied to VIN+, the second signal can be applied to REF and V_{IN}- is ground. The output is equal to Equation 6:

$$V_O = (V_{IN}+ + V_{REF}) \times Gain \quad \text{(EQ. 6)}$$

Also, the EL5172 can be used as a level shifter by applying a level control signal to the REF input.

Revision History

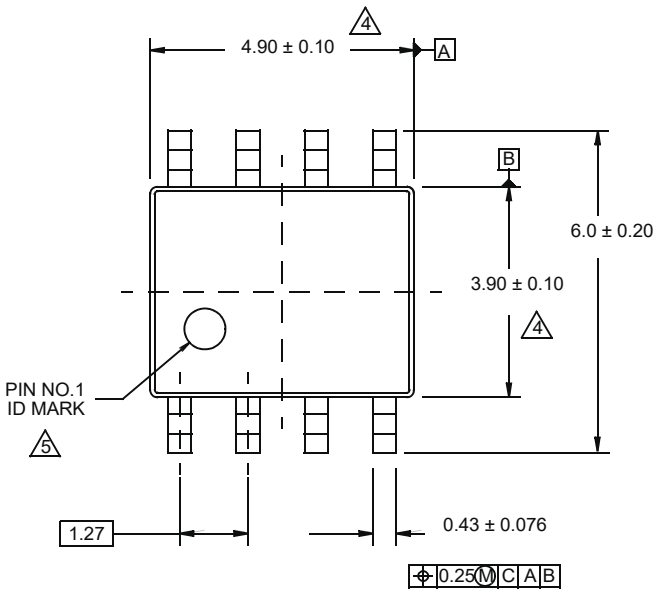
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Jul 30, 2020	12.00	Added Related Literature section. Removed EL5372 information from datasheet. Updated Ordering Information table by adding tape and reel information and updating notes. Added Figure 27. Removed About Intersil section.
Aug 11, 2015	11.00	Updated Ordering Information table on page 2.

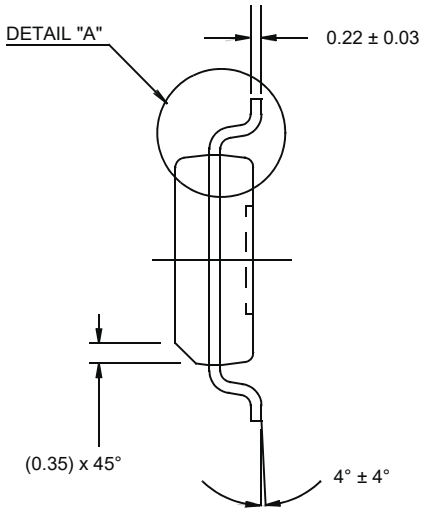
Package Outline Drawings

For the most recent package outline drawing, see M8.15E.

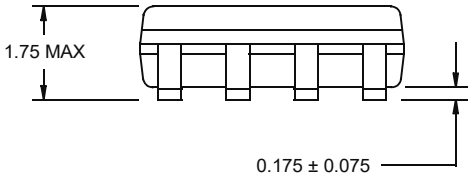
M8.15E
8 Lead Narrow Body Small Outline Plastic Package
Rev 0, 08/09



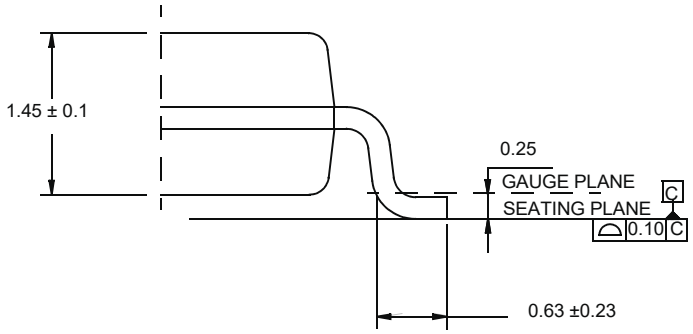
TOP VIEW



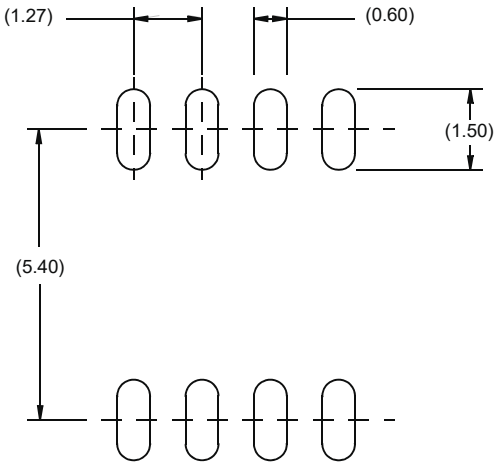
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



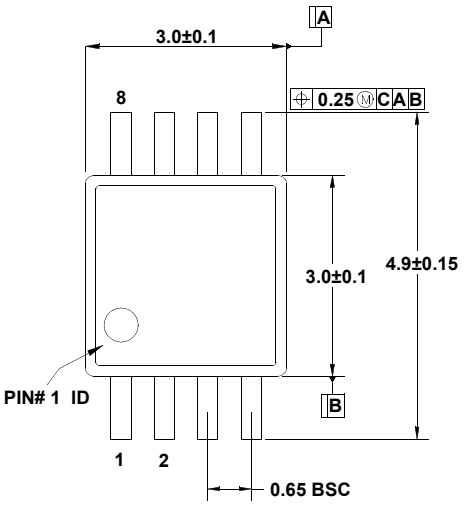
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

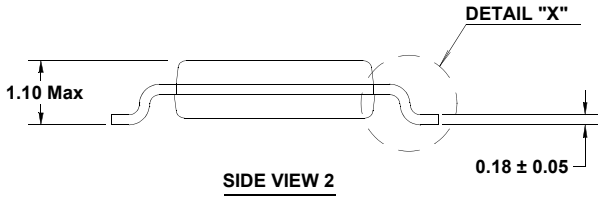
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

M8.118A
8 Lead Mini Small Outline Plastic Package (MSOP)
Rev 0, 9/09

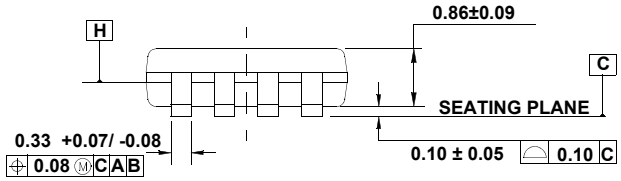
For the most recent package outline drawing, see M8.118A.



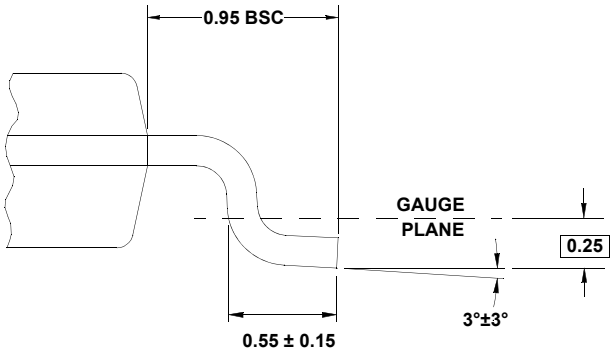
TOP VIEW



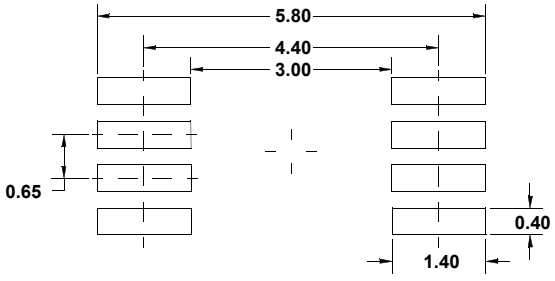
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP 8L.

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(Rev.1.0 Mar 2020)

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