

### FEATURES

**Pretrimmed to  $\pm 0.5\%$  Max 4-Quadrant Error**  
**All Inputs (X, Y and Z) Differential, High Impedance for**  
 $[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$  **Transfer Function**  
**Scale-Factor Adjustable to Provide up to X10 Gain**  
**Low Noise Design: 90  $\mu\text{V}$  rms, 10 Hz–10 kHz**  
**Low Cost, Monolithic Construction**  
**Excellent Long-Term Stability**

### APPLICATIONS

**High Quality Analog Signal Processing**  
**Differential Ratio and Percentage Computations**  
**Algebraic and Trigonometric Function Synthesis**  
**Accurate Voltage Controlled Oscillators and Filters**

### PRODUCT DESCRIPTION

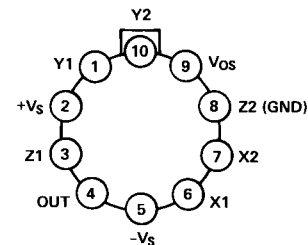
The AD632 is an internally-trimmed monolithic four-quadrant multiplier/divider. The AD632B has a maximum multiplying error of  $\pm 0.5\%$  without external trims.

Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions. The simplicity and flexibility of use provide an attractive alternative approach to the solution of complex control functions.

The AD632 is pin-for-pin compatible with the industry standard AD532 with improved specifications and a fully differential high impedance Z-input. The AD632 is capable of providing gains of up to X10, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD632 can be effectively employed as a variable gain differential input amplifier with high common-mode rejection. The effectiveness of the variable gain capability is enhanced by the inherent low noise of the AD632: 90  $\mu\text{V}$  rms.

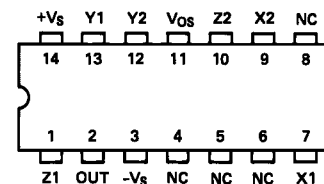
### PIN CONFIGURATIONS

#### H-Package TO-100



#### TOP VIEW

#### D-Package TO-116



#### TOP VIEW

### PRODUCT HIGHLIGHTS

#### Guaranteed Performance Over Temperature

The AD632A and AD632B are specified for maximum multiplying errors of  $\pm 1.0\%$  and  $\pm 0.5\%$  of full scale, respectively at  $+25^\circ\text{C}$  and are rated for operation from  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$ . Maximum multiplying errors of  $\pm 2.0\%$  (AD632S) and  $\pm 1.0\%$  (AD632T) are guaranteed over the extended temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

#### High Reliability

The AD632S and AD632T series are also available with MIL-STD-883 Level B screening and all devices are available in either the hermetically-sealed TO-100 metal can or TO-116 ceramic DIP package.

### REV. A

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# AD632—SPECIFICATIONS (@ +25°C, V<sub>S</sub> = ±15 V, R ≥ 2 kΩ unless otherwise noted)

Model	AD632A			AD632B			AD632S			AD632T			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>MULTIPLIER PERFORMANCE</b>													
Transfer Function	$\frac{(X_1 - X_3)(Y_1 - Y_3) + Z_3}{10V}$			$\frac{(X_1 - X_3)(Y_1 - Y_3) + Z_3}{10V}$			$\frac{(X_1 - X_3)(Y_1 - Y_3) + Z_3}{10V}$			$\frac{(X_1 - X_3)(Y_1 - Y_3) + Z_3}{10V}$			
Total Error <sup>1</sup> (−10 V ≤ X, Y ≤ +10 V)	±1.0			±0.5			±1.0			±0.5			%
T <sub>A</sub> = Min to Max	±1.5			±1.0			±2.0			±1.0			%
Total Error vs. Temperature	±0.022			±0.015			±0.02			±0.01			%/°C
Scale Factor Error (SF = 10.000 V Nominal) <sup>2</sup>	±0.25			±0.1			±0.25			±0.1			%
Temperature-Coefficient of Scaling-Voltage	±0.02			±0.01			±0.2			±0.005			%/°C
Supply Rejection (±15 V ± 1 V)	±0.01			±0.01			±0.01			±0.01			%
Nonlinearity, X (X = 20 V p-p, Y = 10 V)	±0.4			±0.2 ±0.3			±0.4			±0.2 ±0.3			%
Nonlinearity, Y (Y = 20 V p-p, X = 10 V)	±0.2			±0.1 ±0.1			±0.2			±0.1 ±0.1			%
Feedthrough <sup>3</sup> , X (Y Nulled, X = 20 V p-p 50 Hz)	±0.3			±0.15 ±0.3			±0.3			±0.15 ±0.3			%
Feedthrough <sup>3</sup> , Y (X Nulled, Y = 20 V p-p 50 Hz)	±0.01			±0.01 ±0.1			±0.01			±0.01 ±0.1			%
Output Offset Voltage	±5 ±30			±2 ±15			±5 ±30			±2 ±15			mV
Output Offset Voltage Drift	200			100			500			300			μV/°C
<b>DYNAMICS</b>													
Small Signal BW, (V <sub>OUT</sub> = 0.1 rms)	1			1			1			1			MHz
1% Amplitude Error (C <sub>LOAD</sub> = 1000 pF)	50			50			50			50			kHz
Slew Rate (V <sub>OUT</sub> 20 p-p)	20			20			20			20			V/μs
Settling Time (to 1%, ΔV <sub>OUT</sub> = 20 V)	2			2			2			2			μs
<b>NOISE</b>													
Noise Spectral-Density SF = 10 V	0.8			0.8			0.8			0.8			μV/√Hz
SF = 3 V <sup>4</sup>	0.4			0.4			0.4			0.4			μV/√Hz
Wideband Noise A = 10 Hz to 5 MHz	1.0			1.0			1.0			1.0			mV rms
P = 10 Hz to 10 kHz	90			90			90			90			μV/rms
<b>OUTPUT</b>													
Output Voltage Swing	±11			±11			±11			±11			V
Output Impedance (f ≤ 1 kHz)	0.1			0.1			0.1			0.1			Ω
Output Short Circuit Current (R <sub>L</sub> = 0, T <sub>A</sub> = Min to Max)	30			30			30			30			mA
Amplifier Open Loop Gain (f = 50 Hz)	70			70			70			70			dB
<b>INPUT AMPLIFIERS (X, Y and Z)<sup>5</sup></b>													
Signal Voltage Range (Diff. or CM Operating Diff.)	±10 ±12			±10 ±12			±10 ±12			±10 ±12			V V
Offset Voltage X, Y	±5 ±20			±2 ±10			±5 ±20			±2 ±10			mV
Offset Voltage Drift X, Y	100			50			100			150			μV/°C
Offset Voltage Z	±5 ±30			±2 ±15			±5 ±30			±2 ±15			mV
Offset Voltage Drift Z	200			100			500			300			μV/°C
CMRR	60 80			70 90			60 80			70 90			dB
Bias Current	0.8 2.0			0.8 2.0			0.8 2.0			0.8 2.0			μA
Offset Current	0.1			0.1			0.1			0.1			μA
Differential Resistance	10			10			10			10			MΩ
<b>DIVIDER PERFORMANCE</b>													
Transfer Function (X <sub>1</sub> > X <sub>2</sub> )	$10V \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			$10V \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			$10V \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			$10V \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			
Total Error <sup>1</sup> (X = 10 V, −10 V ≤ Z ≤ +10 V)	±0.75			±0.35			±0.75			±0.35			%
(X = 1 V, −1 V ≤ Z ≤ +1 V)	±2.0			±1.0			±2.0			±1.0			%
(0.1 V ≤ X ≤ 10 V, −10 V ≤ Z ≤ 10 V)	±2.5			±1.0			±2.5			±1.0			%
<b>SQUARER PERFORMANCE</b>													
Transfer Function	$\frac{(X_1 - X_2)^2}{10V} + Z_3$			$\frac{(X_1 - X_2)^2}{10V} + Z_3$			$\frac{(X_1 - X_2)^2}{10V} + Z_3$			$\frac{(X_1 - X_2)^2}{10V} + Z_3$			
Total Error (−10 V ≤ X ≤ 10 V)	±0.6			±0.3			±0.6			±0.3			%
<b>SQUARE-ROOTER PERFORMANCE</b>													
Transfer Function, (Z <sub>1</sub> ≤ Z <sub>2</sub> )	$\sqrt{10V(Z_2 - Z_1) + X_2}$			$\sqrt{10V(Z_2 - Z_1) + X_2}$			$\sqrt{10V(Z_2 - Z_1) + X_2}$			$\sqrt{10V(Z_2 - Z_1) + X_2}$			
Total Error <sup>1</sup> (1 V ≤ Z ≤ 10 V)	±1.0			±0.5			±1.0			±0.5			%

Model	AD632A			AD632B			AD632S			AD632T			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY SPECIFICATIONS													
Supply Voltage		±15			±15			±15			±15		V
Rated Performance													V
Operating	±8		±18	±8		±18	±8		±22	±8		±22	V
Supply Current													
Quiescent		4	6		4	6		4	6		4	6	mA

**NOTES**

- <sup>1</sup>Figures given are percent of full-scale, ±10 V (i.e., 0.01% = 1 mV).
- <sup>2</sup>May be reduced to 3 V using external resistor between -V<sub>S</sub> and SF.
- <sup>3</sup>Irreducible component due to nonlinearity; excludes effect of offsets.
- <sup>4</sup>Using external resistor adjusted to give SF = 3 V.
- <sup>5</sup>See functional block diagram for definition of sections.

All min and max specifications are guaranteed.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

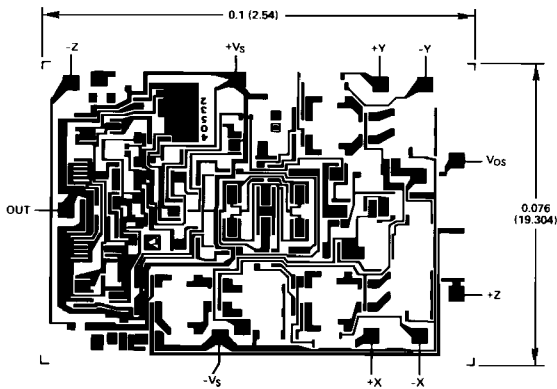
### ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD632AD	-25°C to +85°C	Side Brazed Ceramic DIP	D-14
AD632BD	-25°C to +85°C	Side Brazed Ceramic DIP	D-14
AD632AH	-25°C to +85°C	Header	H-10A
AD632BH	-25°C to +85°C	Header	H-10A
AD632SD	-55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD632SD/833B	-55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD632TD	-55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD632TD/883B	-55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD632SH	-55°C to +125°C	Header	H-10A
AD632SH/883B	-55°C to +125°C	Header	H-10A
AD632TH	-55°C to +125°C	Header	H-10A
AD632TH/883B	-55°C to +125°C	Header	H-10A

\*For outline information see Package Information section.

### CHIP DIMENSIONS AND PAD LAYOUT

Dimensions shown in inches and (mm).  
(Contact factory for latest dimensions.)



For further information, consult factory.

### Thermal Characteristics

Thermal Resistance	$\theta_{JC} = 25^{\circ}\text{C/W}$ for H-10A
	$\theta_{JA} = 150^{\circ}\text{C/W}$ for H-10A
	$\theta_{JC} = 25^{\circ}\text{C/W}$ for D-14
	$\theta_{JA} = 95^{\circ}\text{C/W}$ for D-14

# AD632

## Typical Performance Curves

(typical @ +25°C with  $\pm V_S = 15\text{ V}$ )

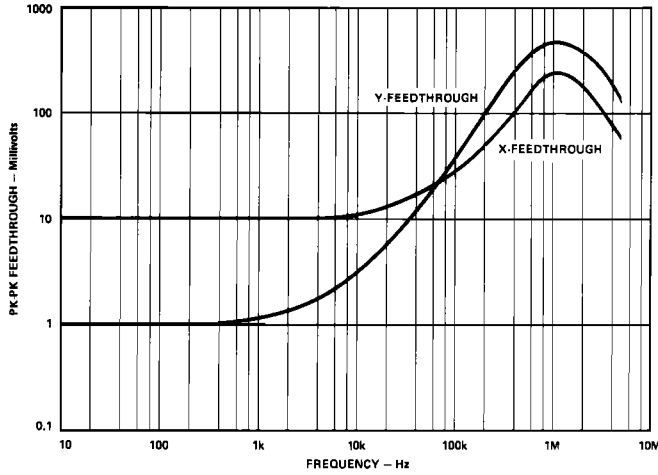


Figure 1. AC Feedthrough vs. Frequency

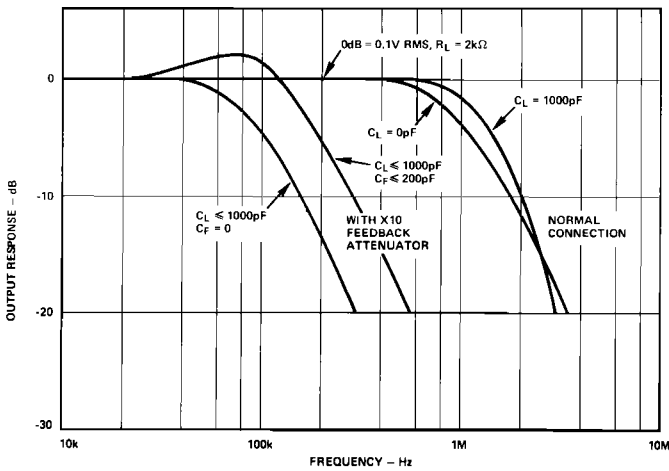


Figure 2. Frequency Response as a Multiplier

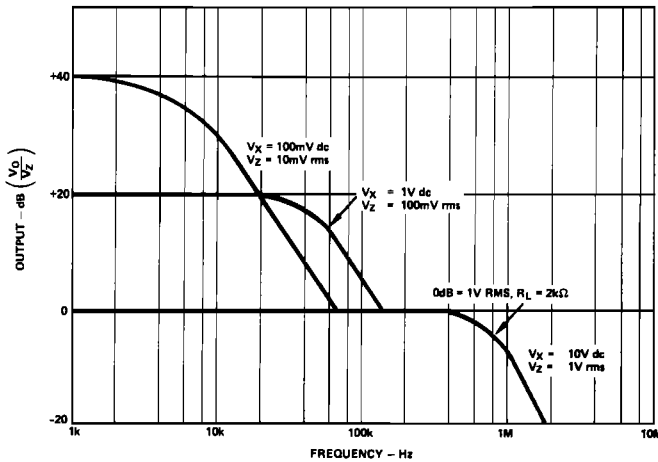


Figure 3. Frequency Response vs. Divider Denominator Input Voltage

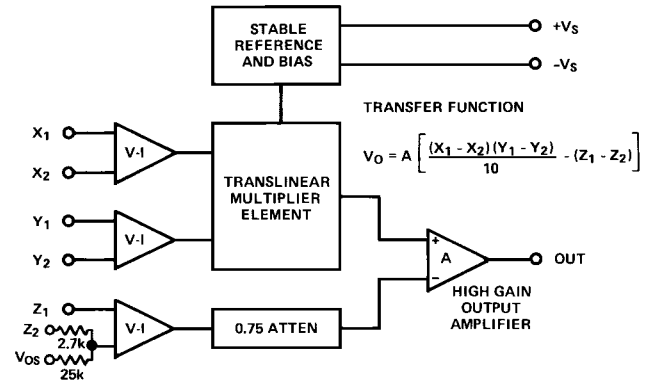


Figure 4. AD632 Functional Block Diagram

### OPERATION AS A MULTIPLIER

Figure 5 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

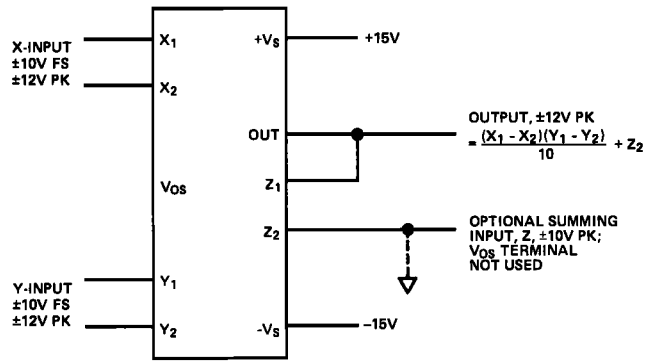


Figure 5. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage ( $\pm 30\text{ mV}$  range required) to the X or Y input. Curve 1 shows the typical ac feedthrough with this adjustment mode. Note that the feedthrough of the Y input is a factor of 10 lower than that of the X input and should be used in applications where null suppression is critical.

The  $Z_2$  terminal of the AD632 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1 MHz small signal bandwidth and a 20 V/ $\mu\text{s}$  slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective signal common potentials to realize the full accuracy of the AD632.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 6. In this example, the scale is such that  $V_{OUT} = XY$ , so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80 kHz without the peaking capacitor  $C_F$ . In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the Z terminal, where they are amplified by  $-10$ , or to the common ground connection where they are amplified by  $-1$ . Input signals may also be applied to the lower end of the  $2.7\text{ k}\Omega$  resistor, giving a gain of  $+9$ .

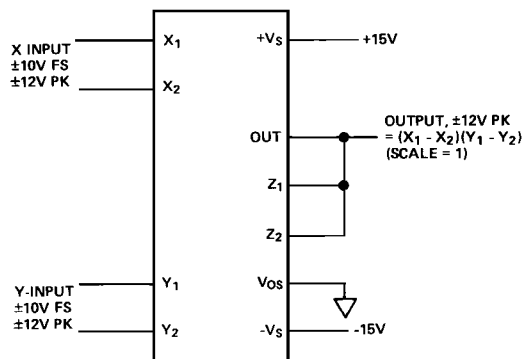


Figure 6. Connections for Scale-Factor of Unity

### OPERATION AS A DIVIDER

Figure 7 shows the connection required for division. Unlike earlier products, the AD632 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to  $Y_1$ . As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in Figure 3.

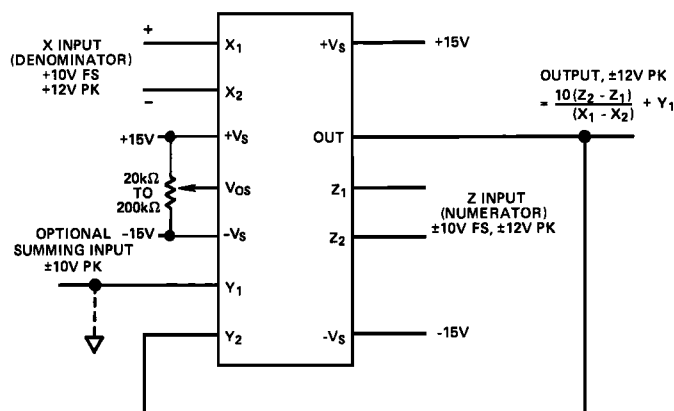


Figure 7. Basic Divider Connection

Without additional trimming, the accuracy of the AD632B is sufficient to maintain a 1% error over a 10 V to 1 V denominator range (The AD535 is functionally equivalent to the AD632 and has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications).

This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is  $\pm 3.5\text{ mV max}$ ) applied to the unused X input. To trim, apply a ramp of  $+100\text{ mV}$  to  $+V$  at  $100\text{ Hz}$  to both  $X_1$  and  $Z_1$  (if  $X_2$  is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.\*

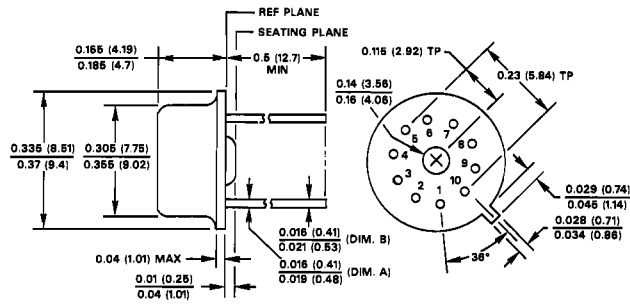
Since the output will be near  $+10\text{ V}$ , it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

\*See the AD535 data sheet for more details.

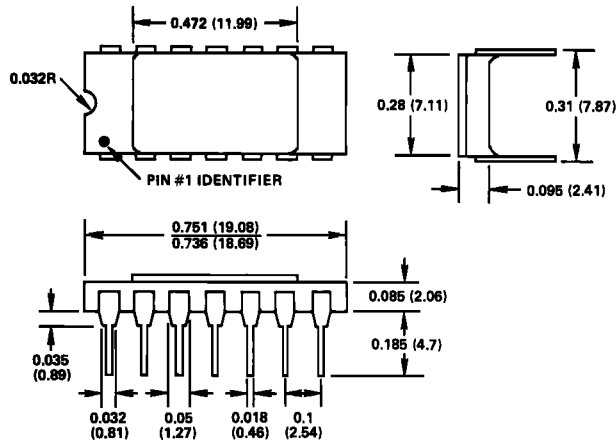
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**H-Package TO-100**



**D-Package TO-116**



C526a-1-6/97

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