Multiple 2 MHz PGAs

AD75062/AD75068

FEATURES

Two or Eight Programmable Gain Amps in a Monolithic IC
Wideband: 2 MHz Bandwidth at All Gain Settings
Low Phase Shift: < 2.5° Up to 10 kHz, < 0.25° Up to 1 kHz
Independent PGA Gains of 1, 2, 4, 8, 16, 32, 64, or 128
Low Nonlinearity: < 0.04% at All Gains
Low Input Bias Current: < 4 pA
Small Size: 16-Pin DIP or 44-Pin JLCC Package
Operates from ±12 V Supplies

APPLICATIONS

Sonar
Instrumentation

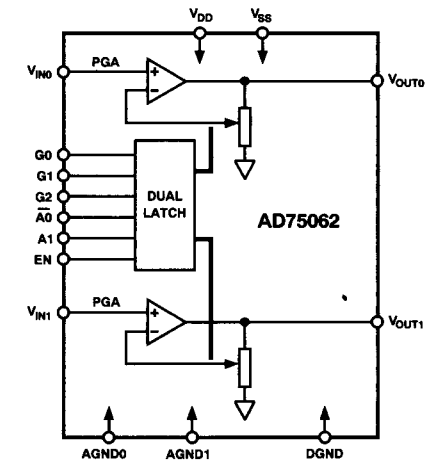
PRODUCT DESCRIPTION

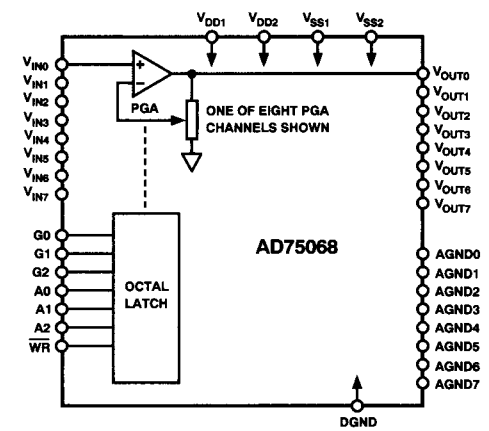
The AD75062 and AD75068 contain multiple programmable-gain amplifiers in one monolithic circuit. The AD75062 has two channels; the AD75068 has eight. Each PGA is complete, including amplifier, gain-setting network, and control latch, and requires no external components. Each PGA may be independently programmed for gains of 1 to 128, in powers of two. A unique circuit design keeps the bandwidth constant at all gains: the −3 dB point is 2 MHz (minimum, small signal).

On-chip voltage regulators for each channel ensure high channel-to-channel isolation (88 dB minimum, dc to 1 kHz) and excellent power supply rejection (65 dB minimum, dc to 10 kHz). To reduce the effects of the impedance of external circuit interconnect between the chip and power supplies, the AD75068 includes two pins for each power supply voltage.

The high performance and functionality of the AD75062 and AD75068 result in part from their fabrication in Analog Devices' BiMOS II process. This epitaxial BiCMOS process features bipolar transistors for precise analog circuitry; CMOS transistors for high impedance inputs, dense logic and analog switches; laser-trimmed thin-film resistors; and double-level metal interconnects.

FUNCTIONAL BLOCK DIAGRAMS





AD75062/AD75068—SPECIFICATIONS (T_A = operating temperature range; V_{DD}, V_{SS} = ±12 V; R_L = 2 kΩ; C_L = 400 pF; unless otherwise noted)

Parameter	AD75062A/AD75068A Min	Typ	Max	Units
GAIN AND GAIN ACCURACY				
Gain Settings (G)		1, 2, 4, 8, 16, 32, 64, 128		V/V
Gain Error				
G = 1 to 16		±0.4	**±1.0**	%
G = 32 or 64		±0.5	**±1.5**	%
G = 128		±1.5	**±2.5**	%
Phase Shift, Input to Output (All Gains)				
f_{IN} = DC to 1 kHz		0.1	0.25	Degree
f_{IN} = DC to 10 kHz		1.0	**2.5**	Degree
Gain Matching Error Between Channels[1]				
G = 1		0.4	**0.75**	%
G = 2 to 128		0.75	**2.0**	%
DYNAMIC RESPONSE				
Small-Signal Bandwidth (V_{OUT} = ±0.5 V, −3 dB)				
All Gains	2	3		MHz
Full-Power Bandwidth (V_{OUT} = ±5.0 V, −3 dB)				
G = 1	100	500		kHz
G = 128	400	1,000		kHz
Settling Time to 0.01 % (ΔV_{OUT} = ±5.0 V)				
G = 1			4	µs
G = 128			2	µs
Gain Change Settling Time to 0.01%				
(V_{OUT} ≤ ±5.0 V, All Gains; See Test Circuit 1)		3.5	4	µs
Slew Rate				
G = 1	5	10		V/µs
G = 128	50	70		V/µs
Overload Recovery Time to 1%				
(V_{IN} = ±5.0 V, All Gains; See Test Circuit 2)			6	µs
NONLINEARITY				
(V_{OUT} = ±4 V)				
G = 1		0.01	**0.04**	% FSR
G = 2 to 32		0.005	**0.01**	% FSR
G = 64		0.01	**0.02**	% FSR
G = 128		0.01	**0.04**	% FSR
(V_{OUT} = ±5 V)				
G = 1		0.1	**0.3**	% FSR
G = 2 to 32		0.005	**0.01**	% FSR
G = 64		0.01	**0.05**	% FSR
G = 128		0.03	**0.07**	% FSR
INPUT CHARACTERISTICS				
Input Bias Current (All Gains, T_A = +25°C)		2	4	pA
Input Bias Current (All Gains, T_A = T_{MIN} to T_{MAX})		60	100	pA
Input Capacitance			20	pF
Input Offset Voltage (G = 1 to 32)		±6	**±20**	mV
Input Offset Voltage (G = 64 or 128)		±4	**±10**	mV
OUTPUT CHARACTERISTICS				
Voltage Range	±5.0			V
Current (Per Channel)	±2.5			mA
CROSSTALK				
Isolation Between Any 2 Channels[2]				
600 Ω‖150 pF Input (See Test Circuit 3)				
DC to 1 kHz	88			dB
10 kHz	73			dB
100 kHz	55			dB
Grounded Input (See Test Circuit 4)				
DC to 100 kHz	100			dB

Parameter	AD75062A/AD75068A Min	Typ	Max	Units
NOISE				
Voltage Noise (RTI, 0.1 Hz to 10 Hz)				
G = 1		7		μV p–p
G = 16		3		μV p–p
G = 128		1		μV p–p
Voltage Noise Density (RTI, G = 1)				
f = 10 Hz		400	650	nV/√Hz
f = 100 Hz		125	180	nV/√Hz
f = 1 kHz		95	125	nV/√Hz
f = 10 kHz		85	110	nV/√Hz
Voltage Noise Density (RTI, G = 128)				
f = 10 Hz		85	170	nV/√Hz
f = 100 Hz		25	45	nV/√Hz
f = 1 kHz		15	35	nV/√Hz
f = 10 kHz		10	12	nV/√Hz
TOTAL HARMONIC DISTORTION				
THD (DC to 10 kHz, ±4 V Output, G = 128)		−83	−75	dB
POWER SUPPLY REJECTION				
PSRR (V_{DD}, V_{SS} = ±11.4 V to ±13.2 V)				
DC	**70**	75		dB
10 kHz	65	70		dB
DIGITAL INPUTS				
Logic "1" Voltage	2		V_{DD}	V
Logic "0" Voltage	0		0.8	V
Logic "1" Current			1	μA
Logic "0" Current			1	μA
POWER SUPPLY REQUIREMENTS				
Voltage Range, V_{DD} and V_{SS}	±11.4	±12	±13.2	V
Supply Current, I_{DD}[3]				
AD75062		14	17	mA
AD75068		42	**66**	mA
Supply Current, I_{SS}[3]				
AD75062		−12	−14	mA
AD75068		−42	**−60**	mA
OPERATING TEMPERATURE				
T_{MIN}, T_{MAX}	−40		+85	°C

NOTES

[1]Gain matching error is determined by finding the maximum, minimum, and average of the gains of all channels on a chip and then calculating: gain matching error = (maximum gain − minimum gain)/(average gain).

[2]Crosstalk isolation is determined by driving one channel with V_{OUT} = ±5 V, R_L = 2 kΩ‖400 pF, G = 1; and measuring a second channel with G = 128.

[3]Maximum supply current occurs when all channels are set to maximum gain. I_{DD} and I_{SS} are measured at V_{DD} and V_{SS} = ±12 V.

All minimum and maximum specifications are guaranteed, and specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

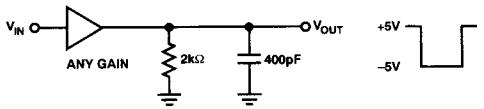
Specifications subject to change without notice.

ORDERING GUIDE

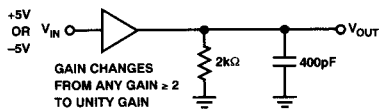
Model	Temperature Range	Number of Channels	Package Description	Package Option*
AD75062AD	−40°C to +85°C	2	Ceramic DIP	D-16
AD75068AJ	−40°C to +85°C	8	Ceramic JLCC	J-44

*For outline information see Package Information section.

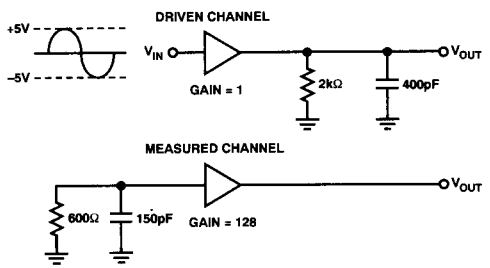
TEST CIRCUITS



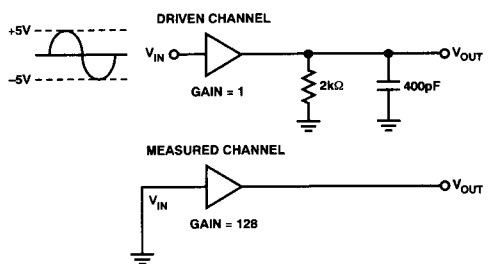
Test Circuit 1. Gain Change Settling Time



Test Circuit 2. Overload Recovery Time



Test Circuit 3. Crosstalk, Ungrounded Inputs

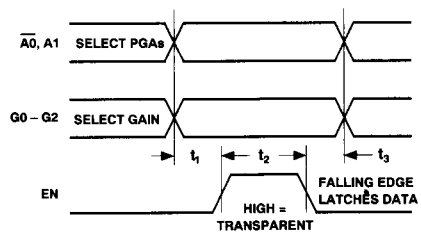


Test Circuit 4. Crosstalk, Grounded Inputs

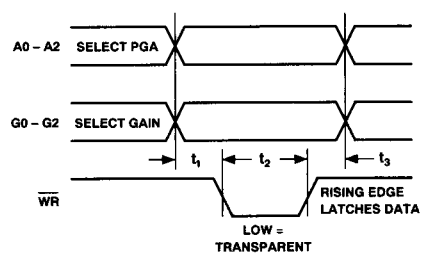
TIMING CHARACTERISTICS[1] (T_A = operating temperature range; V_{DD}, V_{SS} = ±12 V unless otherwise noted)

Parameter	Symbol	Value	Units	Condition
Data Setup Time	t_1	0	ns	min
Write Pulse Width	t_2	80	ns	min
Data Hold Time	t_3	80	ns	min

NOTE
[1]Timing measurement reference level is 1.5 V.
Specifications subject to change without notice.



Timing Diagram 1. AD75062



Timing Diagram 2. AD75068

ABSOLUTE MAXIMUM RATINGS*

(T_A = operating temperature range unless otherwise noted)

V_{DD} to DGND or AGND . . . . . −0.3 V, +18 V
V_{SS} to DGND or AGND . . . . . −18 V, +0.3 V
V_{DD} to V_{SS} . . . . . −0.3 V, +26.4 V
V_{IN} to AGND . . . . . V_{SS}, V_{DD}
Digital Inputs to DGND . . . . . −0.3 V, V_{DD}
AGND to DGND . . . . . −0.3 V, +0.3 V
Power Dissipation ($T_A \leq +85°C$) . . . . . 1.7 W
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Short Circuit Duration . . . . . Indefinite
(Output Connected to Ground, Power Dissipation <max)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The AD75062 and AD75068 have been characterized in accordance with MIL-STD-883C, Method 3015 (Human Body Model), with no degradation in performance observed for levels up to ±1,000 V. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination potential before devices are removed.

CONFIGURING THE AD75062 AND AD75068

The gain of each channel in the AD75062 may be programmed individually or both channels may be set to the same gain simultaneously. To set gains in the AD75062, apply the address(es) to the address inputs and the desired gain value to the gain inputs G0–G2, and then activate the ENable input by pulsing it high. This operation is summarized in Table IA and the timing is illustrated in Timing Diagram 1.

The gain of each channel in the AD75068 is individually programmable. To set the gain of a channel, apply its address to inputs A0–A2 and the desired gain to inputs G0–G2, and then activate the WR/ input by pulsing it low. This operation is summarized in Table IB and the timing is illustrated in Timing Diagram 2.

Table IA. Operation Truth Table—AD75062

Gain Selection			
G2	G1	G0	Gain
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Channel Addressing		
A1	$\overline{A0}$	Channel
0	0	0
0	1	Neither
1	0	Both
1	1	1

Write Modes	
EN	Operation
0	Latched
1	Transparent

Table IB. Operation Truth Table—AD75068

Gain Selection			
G2	G1	G0	Gain
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Channel Addressing			
A2	A1	A0	Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Write Modes	
$\overline{WR}$	Operation
0	Transparent
1	Latched

ANALOG CIRCUIT CONSIDERATIONS

Please refer to the Recommended Circuit Schematics when reading the following section.

Grounding Recommendations

The AD75062 has three pins and the AD75068 has nine pins for analog and digital grounds, designated AGND and DGND. The AGND pins are the ground return pins for the amplifiers. They should be connected to the analog ground point in the system. Any external loads should be returned to system ground.

The DGND pin returns current from the bus interface and logic circuitry of the AD75062/AD75068 to ground. This pin should be connected to the digital ground point in the circuit.

Analog and digital grounds should be connected at one point in the system. If there is a possibility that this connection may be broken or otherwise disconnected, then two diodes should be connected in inverse parallel between the analog and digital ground pins of the AD75062/AD75068 to limit the maximum ground voltage difference.

Power Supplies and Decoupling

The AD75062/AD75068 requires two power supplies for proper operation. V_{DD} and V_{SS} are nominally ±12 V.

Decoupling capacitors should be used on the power supply pins. Good engineering practice dictates locating the bypass capacitors as near as possible to the package pins. Recommended values are 4.7 μF tantalum and 0.1 μF ceramic at each of two places: V_{DD} and V_{SS} to analog ground.

Input Considerations

Input pins have a small amount of capacitance to ground and to adjacent inputs. To maximize bandwidth and minimize crosstalk, each input should be driven by as low a source impedance as possible.

Output Considerations

Each amplifier output can source or sink ±2.5 mA of current to an external load. Short-circuit protection limits load current to a maximum load current of 40 mA. Load capacitance of up to 400 pF can be accommodated with no effect on stability.

Transistor Count

The AD75062 contains 1,170 transistors. The AD75068 contains 4,680 transistors.

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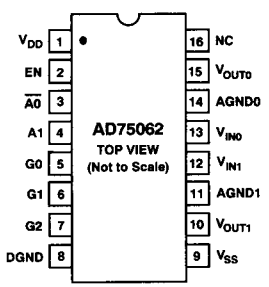
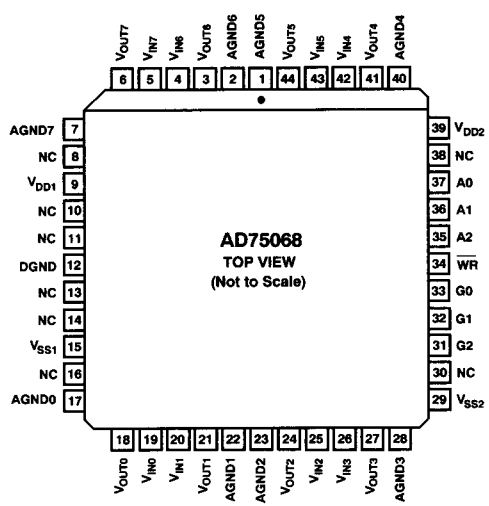
PIN DESCRIPTION—AD75062

Pin	Name	Description
1	V_{DD}	+12 V Power Supply
2	EN	Enable (Active High)
3	$\overline{A0}$	Select Channel 0 (Active Low)
4	A1	Select Channel 1 (Active High)
5	G0	Gain Input Bit 0 (LSB)
6	G1	Gain Input Bit 1
7	G2	Gain Input Bit 2 (MSB)
8	DGND	Digital Ground
9	V_{SS}	−12 V Power Supply
10	V_{OUT1}	Output of PGA 1
11	AGND1	Analog Ground for PGA 1
12	V_{IN1}	Input of PGA 1
13	V_{IN0}	Input of PGA 0
14	AGND0	Analog Ground for PGA 0
15	V_{OUT0}	Output of PGA 0
16	NC	No Internal Connection

PIN CONFIGURATIONS

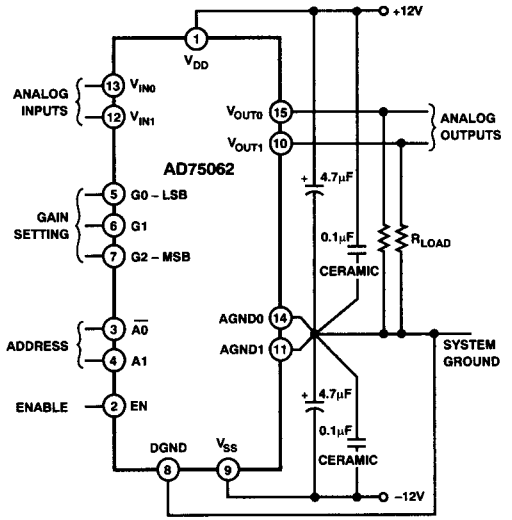




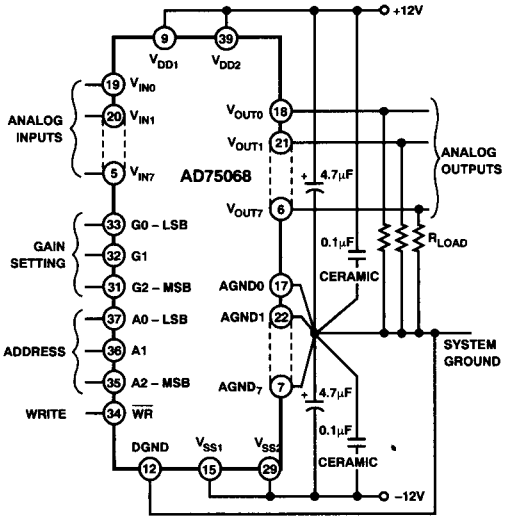
NC = NO INTERNAL CONNECTION

PIN DESCRIPTION—AD75068

Pin	Name	Description
1	AGND5	Analog Ground for PGA 5
2	AGND6	Analog Ground for PGA 6
3	V_{OUT6}	Output of PGA 6
4	V_{IN6}	Input of PGA 6
5	V_{IN7}	Input of PGA 7
6	V_{OUT7}	Output of PGA 7
7	AGND7	Analog Ground for PGA 7
8	NC	No Internal Connection
9	V_{DD1}	+12 V Power Supply
10	NC	No Internal Connection
11	NC	No Internal Connection
12	DGND	Digital Ground
13	NC	No Internal Connection
14	NC	No Internal Connection
15	V_{SS1}	−12 V Power Supply
16	NC	No Internal Connection
17	AGND0	Analog Ground for PGA 0
18	V_{OUT0}	Output of PGA 0
19	V_{IN0}	Input of PGA 0
20	V_{IN1}	Input of PGA 1
21	V_{OUT1}	Output of PGA 1
22	AGND1	Analog Ground for PGA 1
23	AGND2	Analog Ground for PGA 2
24	V_{OUT2}	Output of PGA 2
25	V_{IN2}	Input of PGA 2
26	V_{IN3}	Input of PGA 3
27	V_{OUT3}	Output of PGA 3
28	AGND3	Analog Ground for PGA 3
29	V_{SS2}	−12 V Power Supply
30	NC	No Internal Connection
31	G2	Gain Input Bit 2 (MSB)
32	G1	Gain Input Bit 1
33	G0	Gain Input Bit 0 (LSB)
34	$\overline{WR}$	Write Input; Active Low
35	A2	Address Input 2 (MSB)
36	A1	Address Input 1
37	A0	Address Input 0 (LSB)
38	NC	No Internal Connection
39	V_{DD2}	+12 V Power Supply
40	AGND4	Analog Ground for PGA 4
41	V_{OUT4}	Output of PGA 4
42	V_{IN4}	Input of PGA 4
43	V_{IN5}	Input of PGA 5
44	V_{OUT5}	Output of PGA 5



Recommended Circuit Schematic – AD75062



Recommended Circuit Schematic – AD75068

OPERATING PRINCIPLES

To maintain a fixed closed-loop bandwidth, each channel's amplifier input-stage transconductance changes as its gain setting changes. This is done by engaging more PMOS devices in parallel to form the input stage: with the gain set to 1×, two devices make up the input stage; at a gain of 8×, 16 devices; finally, with gain set to 128×, 256 devices operate in parallel. When the gain is set to 1×, approximately 20 μA flow in the input stage; at a gain of 128, about 3 mA flow.

The noise and input offset specifications reflect this input-stage design. Generally, the input offset falls as the gain is increased, due to the averaging effect of more devices in the input stage. The input noise will fall also, since it has a thermal component proportional to the square root of the input transresistance. As the gain increases, more devices are paralleled, the active gate area increases, and the 1/f noise component decreases. The input capacitance and leakage are not affected by gain changes, because the sources of the PMOS devices are switched, not their gates.

The AD75062/AD75068 is a conventional two-stage amplifier in other respects. An output integrator with a fixed-value capacitor sets the bandwidth. Because the input-stage current increases with gain, the amplifier's slew rate greatly increases and the settling time decreases at higher gains. Furthermore, the full-power bandwidth is almost constant for gains from 1× to 128×.

To give high channel-to-channel isolation and good power-supply rejection, the chip individually regulates the supplies to each amplifier. These regulators require some voltage headroom, so the input and output voltage ranges are restricted to ±5 volts at low supply voltages (±11.4 V).

THERMAL DESIGN CONSIDERATIONS—AD75068

The AD75068, due to its wide gain-independent bandwidth and high integration, may dissipate up to 1.6 W of power in certain operating modes. The reliability of the AD75068 will be significantly enhanced by keeping it as cool as possible, and by not exceeding the maximum junction temperature of 175°C.

Certain applications may require an external heatsink, forced air, or other cooling.

The power dissipation of the AD75068 is a function of the gains selected for all of the channels. The worst-case power dissipation (P_D) can be estimated from this equation:

$$P_D = 600\ mW + \sum_{ch=0}^{7} (G_{CH} \times 1\ mW)$$

where G_{CH} is the gain (1, 2, 4, 8, 16, 32, 64, or 128) of the respective channel (0 through 7). With all eight channels set at minimum (1 ×) gain, the AD75068 will typically dissipate less than 600 mW. For each doubling of gain, the gain-dependent portion of the power dissipation per channel will also double. For example, if all channel gains are set to 2 ×, the power dissipation could increase to 600 mW + 8 × (2 × 1 mW) = 616 mW. If all channels are operated at maximum gain (128×), the power dissipation could increase to 600 mW + 8 × (128 × 1 mW) = 1.62 W.

The junction temperature of the device in a specific application can be computed from the thermal resistance of the package and the estimated power dissipation, e.g.,

$$T_{JUNCTION}\ [°C] = T_{AMBIENT}\ [°C] + P_D\ [W] \times \theta_{JA}\ [°C/W]$$

or

$$T_{JUNCTION}\ [°C] = T_{CASE}\ [°C] + P_D\ [W] \times \theta_{JC}\ [°C/W]$$

where θ_{JA} is the junction-ambient and θ_{JC} is the junction-case thermal resistance.

The actual thermal resistance depends on the mounting configuration of the device and the air flow over it. The thermal resistance of the AD75068 has been measured in the following conditions for devices soldered to a printed-wiring board operating near the maximum power dissipation, with and without a heatsink. The heatsink was an EG&G Wakefield Engineering part #651-B (6 × 10 × 19 mm) attached with cyanoacrylate adhesive.

Table II. AD75068 Thermal Resistance

Condition	Thermal Resistance (°C/W)	
	θ_{JA}	θ_{JC}
Without Heatsink		
Still Air	40	17
200 lfpm	30	15
With Heatsink		
Still Air	37	14
200 lfpm	24	10
400 lfpm	19	8
600 lfpm	17	7
800 lfpm	15	7

The data in the above table is graphed in Figure 1.

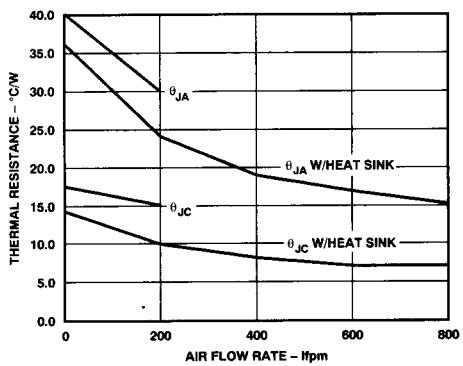


Figure 1. Thermal Resistance

The reliability of the AD75062/AD75068, as measured by the mean-time-to-failure (MTTF), is directly dependent on the junction temperature. The MTTF will increase by approximately 50% for each 13°C decrease in junction temperature, as shown in Figure 2 below. This calculation was based on Military Handbook 217E, "Reliability Prediction of Electronic Equipment."

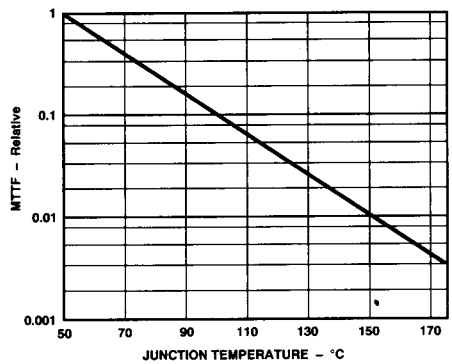


Figure 2. Relative Reliability vs. Temperature