

LINEAR SYSTEMS

Twenty-Five Years Of Quality Through Innovation

LS840 LS841 LS842

LOW NOISE LOW DRIFT
LOW CAPACITANCE
MONOLITHIC DUAL N-CHANNEL JFET

FEATURES

LOW NOISE	$e_n=8\text{nV}/\text{Hz}$ TYP.
LOW LEAKAGE	$I_G=10\text{pA}$ TYP.
LOW DRIFT	$ V_{GS1-2}/T = 5\mu\text{V}/^\circ\text{C}$ max.
LOW OFFSET VOLTAGE	$ V_{GS1-2} = 2\text{mV}$ TYP.

ABSOLUTE MAXIMUM RATINGS¹

@ 25°C (unless otherwise noted)

Maximum Temperatures

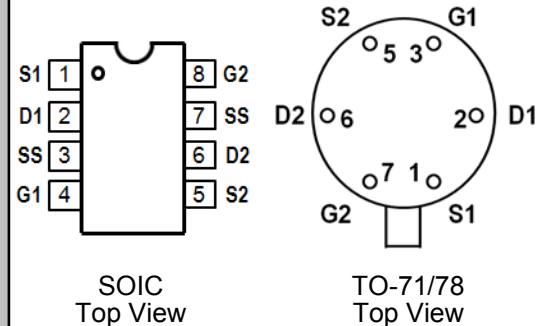
Storage Temperature	-55°C to +150°C
Operating Junction Temperature	-55°C to +150°C

Maximum Voltage and Current for Each Transistor¹

$-V_{GSS}$	Gate Voltage to Drain or Source	60V
$I_{G(f)}$	Gate Forward Current	10mA

Maximum Power Dissipation

Device Dissipation ² @ Free Air - Total	400mW $T_A=+25^\circ\text{C}$
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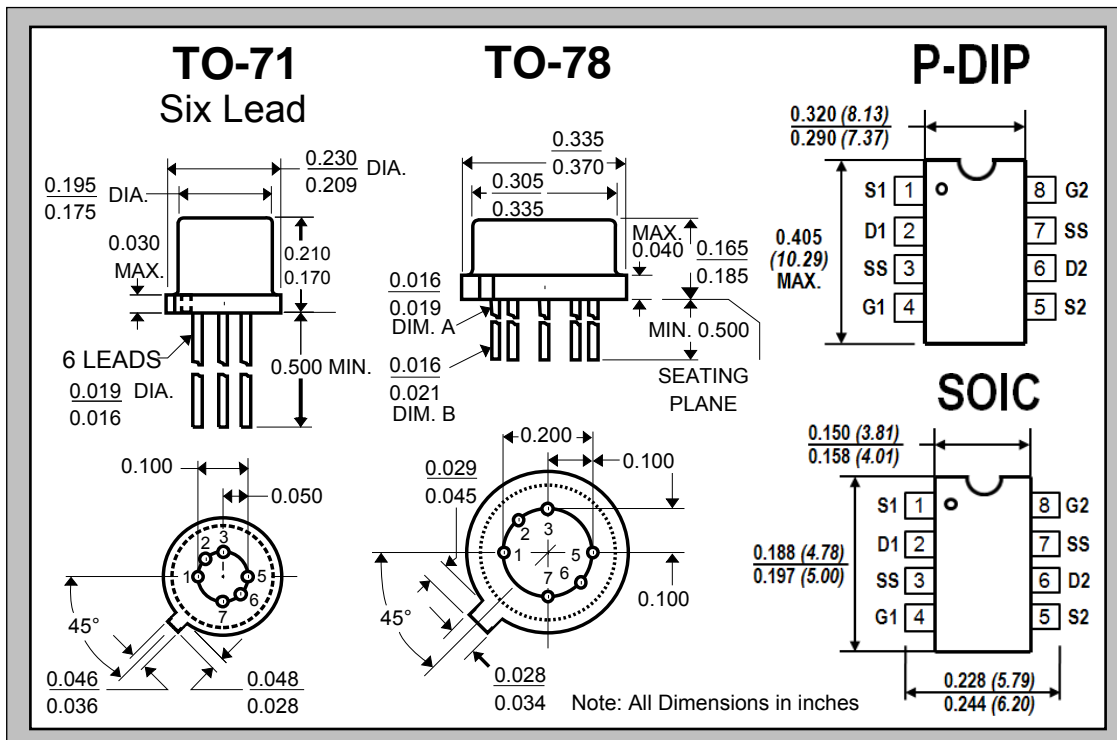


ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS840	LS841	LS842	UNITS	CONDITIONS
$ V_{GS1-2}/T $ max.	Drift vs. Temperature	5	10	40	$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$
$ V_{GS1-2} $ max.	Offset Voltage	5	10	25	mA	$V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$

SYMBOL	CHARACTERISTIC ³	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-60	--	--	V	$V_{DS} = 0$ $I_D = -1\text{nA}$
BV_{GGO}	Gate-to-Gate Breakdown	± 60	--	--	V	$I_{GGO} = \pm 1\mu\text{A}$ $I_D = 0$ $I_S = 0$
TRANSCONDUCTANCE						
G_{fss}	Full Conduction	1000		4000	μS	$V_{DG} = 20\text{V}$ $V_{GS} = 0$ $f = 1\text{kHz}$
G_{fs}	Typical Conduction	500		1000	μS	$V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$
$\frac{G_{fs1}}{G_{fs2}}$ ⁴	Mismatch Transconductance Ratio	0.97		1.0		
DRAIN CURRENT						
I_{DSS}	Full Conduction	0.5	2	5	mA	$V_{DG} = 20\text{V}$ $V_{GS} = 0$
$\frac{I_{DSS1}}{I_{DSS2}}$ ⁴	Drain Current Ratio	0.95		1.0		
GATE-SOURCE						
$V_{GS(off)}$	Pinchoff Voltage	-1	-2	-4.5	V	$V_{DS} = 20\text{V}$ $I_D = 1\text{nA}$
V_{GS}	Operating Range	-0.5	--	-4	V	$V_{DS} = 20\text{V}$ $I_D = 200\mu\text{A}$
GATE CURRENT						
$-I_G$	Operating	--	10	50	pA	$V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$
$-I_G$	High Temperature	--	--	50	nA	$V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$ $T_A = +125^\circ\text{C}$
$-I_G$	Reduced VDG	--	5	--	pA	$V_{DG} = 10\text{V}$ $I_D = 200\mu\text{A}$
$-I_{GSS}$	At Full Conduction	--	--	100	pA	$V_{DG} = 20\text{V}$ $V_{DS} = 0$

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
G_{OSS}	OUTPUT CONDUCTANCE					
	Full Conduction	--	--	10	μS	$V_{DS}=20V$ $V_{GS}=0$
	Operating	--	0.1	1	μS	$V_{DS}=20V$ $I_D=200\mu A$
$ G_{OS1-2} $	Differential	--	0.01	0.1	μS	
CMRR	COMMON MODE REJECTION					
	$-20 \log V_{GS1-2}/V_{DS} $	--	100	--	dB	$V_{DS}=10$ to $20V$ $I_D=200\mu A$
CMRR		--	75	--	dB	$V_{DS}=5$ to $10V$ $I_D=200\mu A$
NF	NOISE					
	Figure	--	--	0.5	dB	$V_{DS}=20V$ $V_{GS}=0$ $R_G=10M$ $f=100Hz$ $NBW=6Hz$
e_n	Voltage	--	--	10	nV/Hz	$V_{DS}=20V$ $I_D=200\mu A$ $f=1KHz$ $NBW=1Hz$
e_n	Voltage	--	--	15	nV/Hz	$V_{DS}=20V$ $I_D=200\mu A$ $f=10Hz$ $NBW=1Hz$
C_{ISS}	CAPACITANCE					
	Input	--	4	10	pF	$V_{DS}=20V$ $I_D=200\mu A$
	Reverse Transfer	--	1.2	5	pF	
C_{DD}	Drain-to-Drain	--	0.1	--	pF	$V_{DG}=20V$ $I_D=200\mu A$



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired
2. Derate 4mW/°C above 25°C
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate electrical polarity only.
4. Assumes smaller number in the numerator.

Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, co-founder and vice president of R&D at Intersil, and founder/president of Micro Power Systems.