Clock Generator for PowerQUICC and PowerPC Microprocessors and Microcontrollers

MPC9824

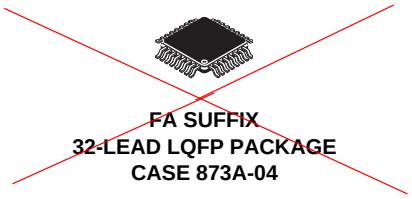
PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES SEPTEMBER 7, 2016

DATASHEET

The MPC9824 is a PLL based clock generator specifically designed for Freescale Microprocessor and Microcontroller applications including the PowerPC and PowerQUICC. This device generates the microprocessor input clock and other microprocessor system and bus clocks at any one of eight output frequencies. These frequencies include 33, 50, 66, 100, 125, 133.33, 166.66 and 200 MHz. The device offers six low skew clock outputs plus the three reference outputs. The clock input reference is 25 MHz and may be derived from an external source of by the addition of a 25 MHz crystal to the on-chip crystal oscillator. The extended temperature range of the MPC9824 supports telecommunication and networking requirements.

MPC9824

MICROPROCESSOR CLOCK GENERATOR



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-04

AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-04

Features

- 6 LVCMOS outputs for processor and other system circuitry
- 3 Buffered 25 MHz reference clock outputs
- Crystal oscillator or external reference input
- 25 MHz Input reference frequency
- Selectable output frequencies = 33.33, 50, 66.66, 100, 125, 133.33, 166.66, or 200 MHz
- Low cycle-to-cycle and period jitter
- Package = 32 lead LQFP
- 3.3 V supply
- Supports computing, networking, telecommunications applications
- Ambient temperature range -40°C to +85°C
- For functional replacement use 8T49N285A

Functional Description

The MPC9824 uses a PLL with a 25 MHz input reference frequency to generate a single bank of 6 configurable LVCMOS output clocks. The output frequency of this bank is configurable by three FSEL pins. The 25 MHz reference may be either an external frequency source or a 25 MHz crystal. The 25 MHz crystal is directly connected to the XTAL_IN and XTAL_OUT pins with no additional components required. An external reference may be applied to the XTAL_IN pin with the XTAL_OUT pin left floating. The input reference, whether provided by a crystal or an external input is also directly buffered to a second bank of 3 LVCMOS outputs. These outputs may be used as the clock source for processor I/O applications such as an Ethernet PHY.

The MPC9824 is packaged in a 32 lead LQFP package.

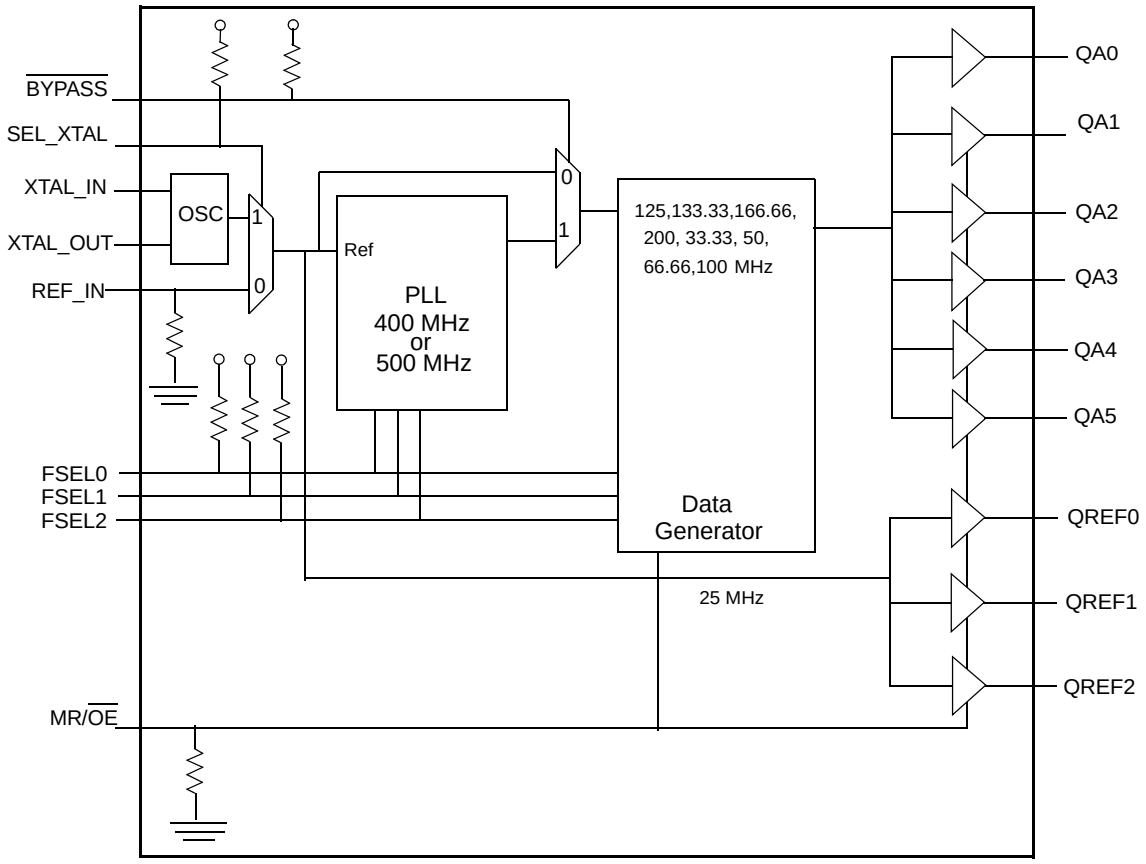


Figure 1. MPC9824 Logic Diagram

Table 1. Pin configuration

Pin	I/O	Type	Function
QA0, QA1, QA2 QA3, QA4, QA5	Output	LVCMOS	Clock Outputs
QREF0, QREF1, QREF2	Output	LVCMOS	Reference Output (25 MHz)
XTAL_IN	Input	LVCMOS	Crystal Oscillator Input Pin
XTAL_OUT	Output	LVCMOS	Crystal Oscillator Output Pin
REF_IN	Input	LVCMOS	External Reference Input (internal pull-down)
SEL_XTAL	Input	LVCMOS	Selects between XTAL or External Source (internal pull-up)
FSEL0 FSEL1 FSEL2	Input	LVCMOS	Configures Bank A Clock Output Frequency (internal pull-up)
$\overline{\text{BYPASS}}$	Input	LVCMOS	Test Mode to Bypass PLL (active low, internal pull-up)
MR/$\overline{\text{OE}}$	Input	LVCMOS	Master Reset (internal pull-down)
V_{DDA}			Analog Supply, An external filter is recommended
V_{DD}	—	—	3.3 V Supply
GND	—	—	Ground

Table 2. FSEL Function Table

FSEL0	FSEL1	FSEL2	VCO Frequency	Output Frequency
0	0	0	400	33.33 MHz
0	0	1	400	66.66 MHz
0	1	0	400	50 MHz
0	1	1	400	100 MHz
1	0	0	500	125 MHz
1	0	1	500	166.66 MHz
1	1	0	400	133.33 MHz
1	1	1	400	200 MHz

Table 3. Function Table

Control	0	1
SEL_XTAL	External Reference	Crystal Input
$\overline{\text{BYPASS}}$	PLL Bypassed	Normal Operation
MR/$\overline{\text{OE}}$	Normal	Reset

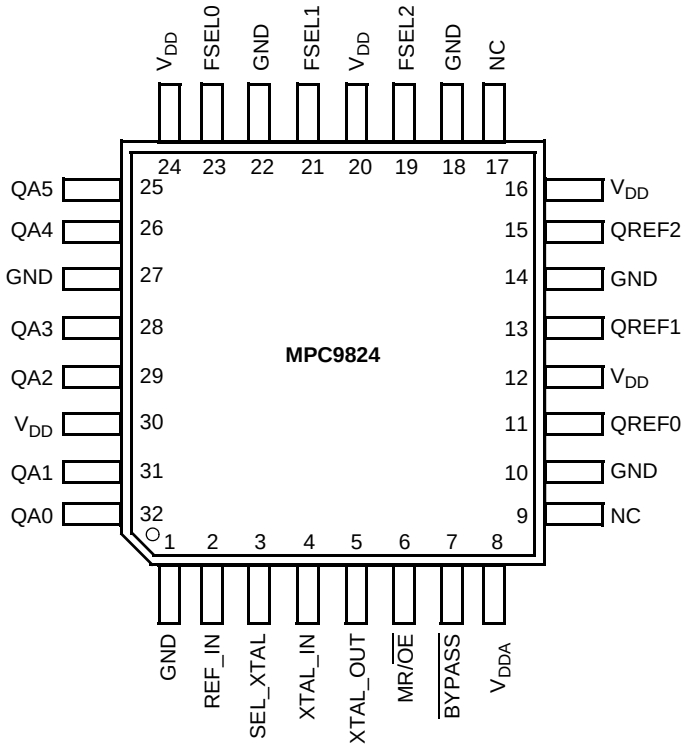


Figure 2. MPC9824 32-Lead LQFP Package Pinout (Top View)

MPC9824 OPERATION

Crystal Oscillator

The MPC9824 features a fully integrated Pierce oscillator to minimize system implementation costs. The MPC9824 may be operated with a 25 MHz crystal without other components. For operation without external components, the crystal selection should be of a 25 MHz parallel resonant type with a load specification of CL = 10 pF. See Table 4 for complete crystal specifications.

If more precise frequency control is desired, the addition of capacitors from each of the XTAL_IN and XTAL_OUT pins to ground may be used to trim the frequency as shown in Figure 3. In this case the recommended crystal should have a CL = 18 pF.

In either case the crystal should be located as close to the MPC9824 XTAL_IN and XTAL_OUT pins as possible to minimize any board level parasitic capacitance.

Table 4. Crystal Specifications

Parameter	Value	Value (with trim caps)
Crystal Cut	Fundamental AT Cut	Fundamental AT Cut
Resonance	Parallel Resonance	Parallel Resonance
Shunt Capacitance (C_O)	5–7 pF	5–7 pF
Load Capacitance (C_L)	18 pF	18 pF
Equivalent Series Resistance (ESR)	20–50 Ω	20–50 Ω

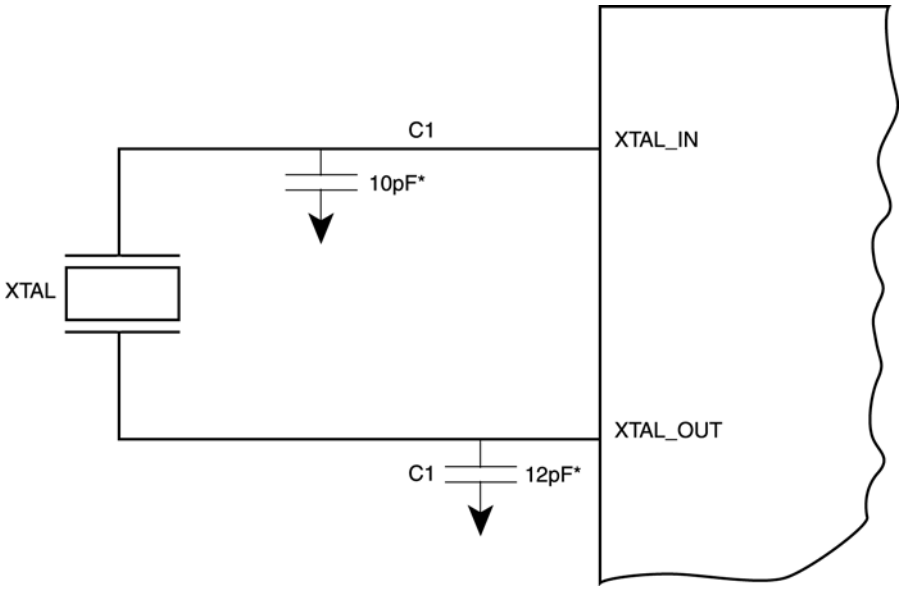


Figure 3 Crystal with Trim Caps

*NOTE: These are recommended values and are subject to change due to specific crystal paramter and board layout. Refer to ICS Application Notes for futher information on the crystal selection.

Power-Supply Bypassing

The MPC9824 should have all V_{DD} pins bypassed with 0.01 µF capacitors and a minimum of one 1.0 µF capacitor for the overall package. All capacitors should be located as close to the package as possible.

An external RC filter from V_{DD} to V_{DDA} is recommended as shown in Figure 4.

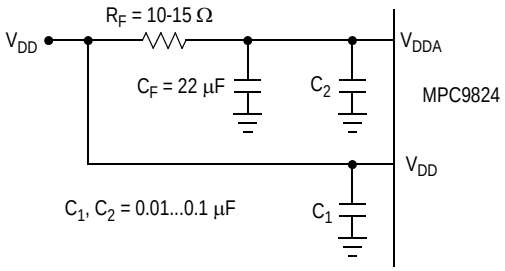


Figure 4. Power Supply Filter

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{DD}	Supply Voltage	–0.3	3.8	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±75	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{DD} \div 2$		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4		pF	Inputs
T_C	Ambient Temperature	–40		85	°C	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
R_{PU}, R_{PD}	Pull-up/Pull-down Resistance			75	KΩ	

Table 7. DC Characteristics (V_{DD} = 3.3 V ± 5%, T_A = –40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage (xtal_in)	2.4		V_{DD} + 0.3	V	Input threshold = V_{DD}/2
V_{IH}	Input High Voltage	2.0		V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[1]			±150	µA	V_{IN} = V_{DD} or GND
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –12 mA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 12 mA
Z_{OUT}	Output Impedance		14		Ω	
I_{DD}	Maximum Quiescent Supply Current			3.5	mA	V_{DD} pins, output not loaded
I_{DDA}	Maximum Quiescent Supply Current			6.5	mA	V_{DDA} pins, output not loaded

1. Inputs have pull-down or pull-down resistors affecting the input current.

Table 8. AC Characteristics (V_{DD} = 3.3 V ± 5%, T_A = –40°C to +85°C) [1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Input and Output Timing Specification						
f_{ref}	Input Reference Frequency (25 MHz input) XTAL Input		25 25		MHz MHz	
f_{VCO}	VCO Frequency Range FSEL0, FSEL1, FSEL2 = 000,001, 010,011,110,111 FSEL0, FSEL1, FSEL2 = 100,101		 400 500		MHz	
f_{MCX}	Output Frequency (QAx) FSEL0, FSEL1, FSEL2 = 000 FSEL0, FSEL1, FSEL2 = 001 FSEL0, FSEL1, FSEL2 = 010 FSEL0, FSEL1, FSEL2 = 011 FSEL0, FSEL1, FSEL2 = 100 FSEL0, FSEL1, FSEL2 = 101 FSEL0, FSEL1, FSEL2 = 110 FSEL0, FSEL1, FSEL2 = 111 Output Frequency (QREFx)		 33.33 66.66 50 100 125 166.66 133.33 200 25		 MHz	PLL locked
DC	Output Duty Cycle	45	50	55	%	
f_{out}	Output Frequency Accuracy Crystal[2] External Reference	 0		 100 0	 ppm ppm	
PLL Specifications						
BW	PLL Closed Loop Bandwidth[3]		500		kHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	
Skew and Jitter Specifications						
$t_{sk(O)}$	Output-to-Output Skew			100	ps	within bank
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter			100	ps	QA output
$t_{JIT(PER)}$	Period Jitter			75	ps	QA output
$t_{JIT(Ø)}$	I/O Phase Jitter, RMS			30	ps	
t_r, t_f	Output Rise/Fall Time			750	ps	20% to 80%
t_{JIT}	Phase Noise Jitter, RMS; 25MHz, Integration Range: 1.875MHz - 20MHz			2.5	ps	QREF pin

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. Based upon recommended crystal specifications and tune-in capacitors as outlined in operation section..
3. dB point of PLL transfer characteristics.

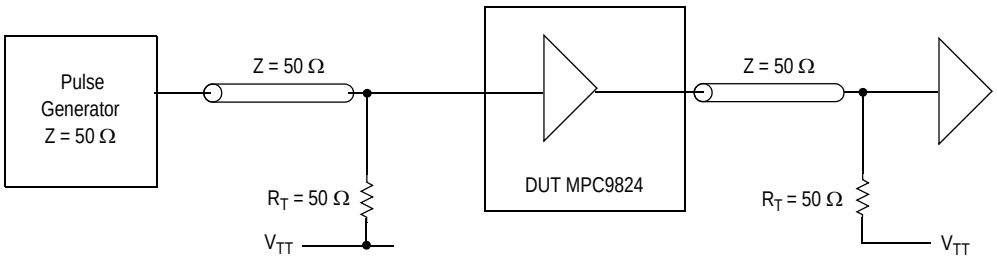


Figure 5. MPC9824 AC Test Reference (LVCMOS Outputs)

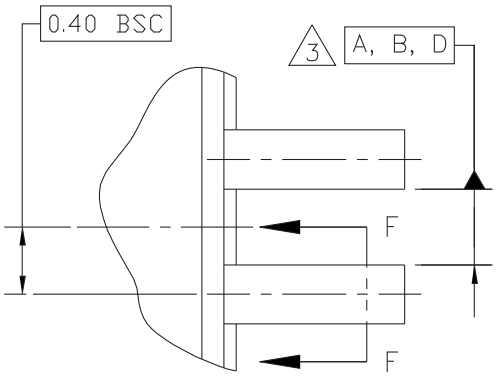
RELIABILITY INFORMATION

Table 9. θ_{JA} vs. Air Flow Table for 32 Lead LQFP

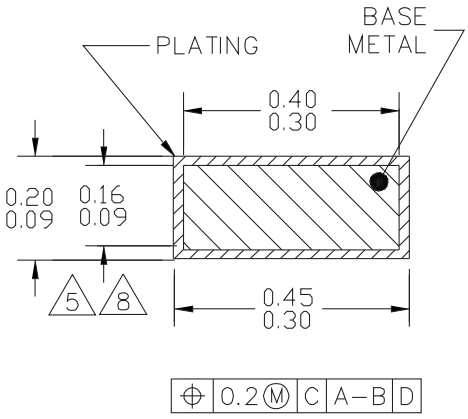
θ_{JA} BY VELOCITY (LINEAR FEET PER MINUTE)			
	0	200	500
Single-Laye PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

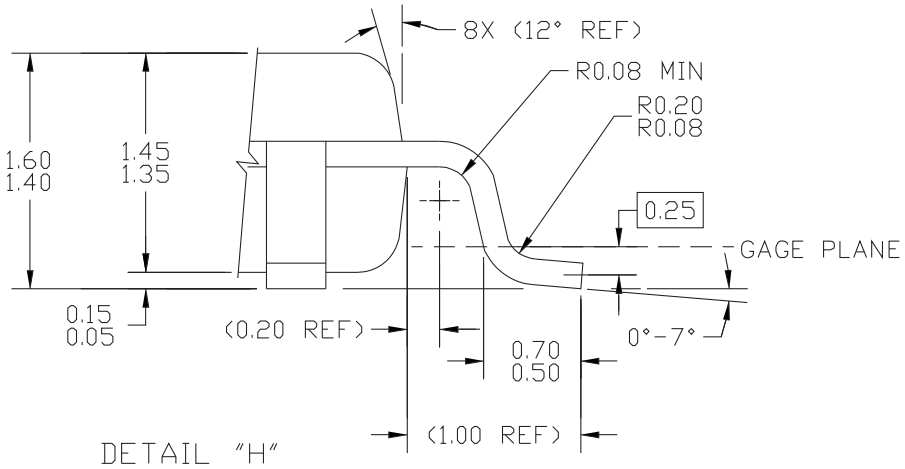
PACKAGE DIMENSIONS



DETAIL G



SECTION F–F
ROTATED 90°CW
32 PLACES



DETAIL "H"

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TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: C
	CASE NUMBER: 873A-04	01 APR 2005
	STANDARD: JEDEC MS-026 BBA	

CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.

3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70029A	REV: C
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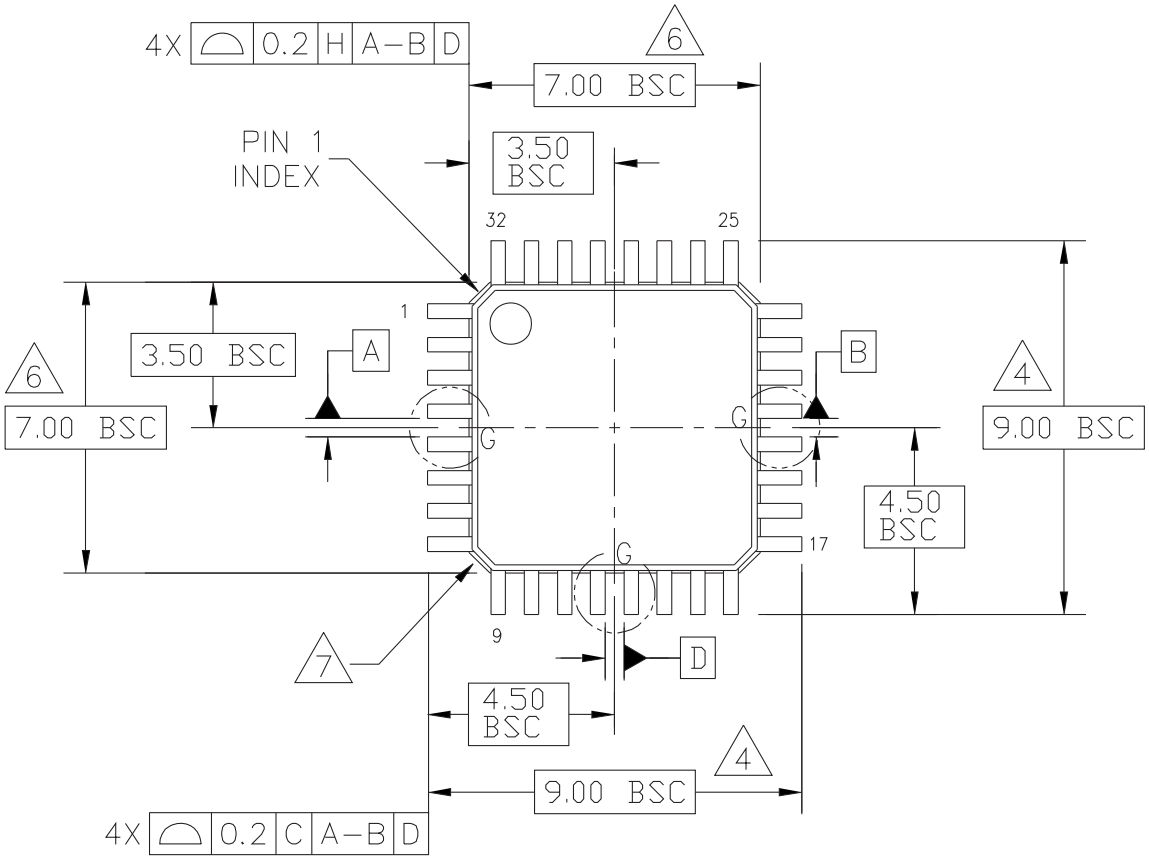
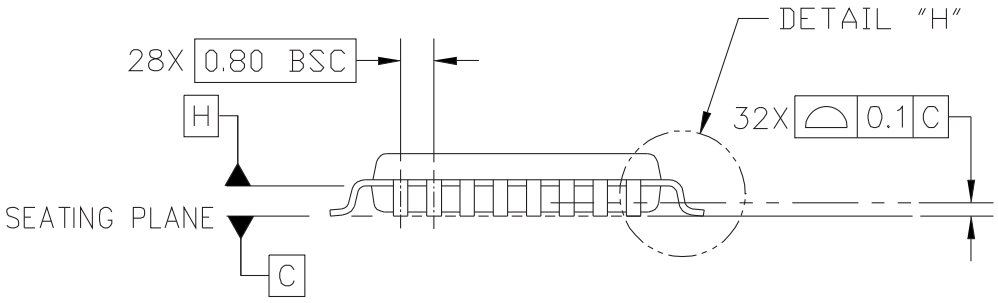
CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE

PACKAGE DIMENSIONS





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CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE

Revision History Sheet

Rev	Table	Page	Description of Change	Date
2		1	NRND – Not Recommend for New Designs	2/15/2013
2		1	Removed NRND.	5/5/15
2		1	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02	3/16/16

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