

<b>NOTICE OF REVISION (NOR)</b>		1. DATE (YYMMDD) 96-10-31	Form Approved OMB No. 0704-0188
THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.			
<small>Public reporting burden for this collection is estimated to average 2 hours per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503. PLEASE DO NOT RETURN YOUR COMPLETED FORM TO EITHER OF THESE ADDRESSES. RETURN COMPLETED FORM TO THE GOVERNMENT ISSUING CONTRACTING OFFICER FOR THE CONTRACT/PROCURING ACTIVITY NUMBER LISTED IN ITEM 2 OF THIS FORM.</small>		2. PROCURING ACTIVITY NO.	
		3. DODAAC	
4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code) Defense Supply Center Columbus 3990 East Broad Street Columbus, OH 43216-5000	5. CAGE CODE 67268	6. NOR NO. 5962-R056-97
a. TYPED NAME (First, Middle Initial, Last)		7. CAGE CODE 67268	8. DOCUMENT NO. <b>5962-89681</b>
9. TITLE OF DOCUMENT MICROCIRCUIT, LINEAR, OCTAL GENERAL INTERFACE BUS TRANSCEIVER, MONOLITHIC SILICON		10. REVISION LETTER	
		a. CURRENT B	b. NEW C
11. ECP NO.  Record of verbal coordination on file			
12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES All			
13. DESCRIPTION OF REVISION			
<p>Sheet 1: Revisions ltr column; add "C".  Revisions description column; add "Changes in accordance with NOR 5962-R056-97".  Revisions date column; add "96-10-31".  Revision level block; change from "B" to "C".  Rev status of sheets; for sheets 1, 5, and 6 change from "B" to "C".</p> <p>Sheet 5: Table I; for propagation delay time test (<math>t_{PHL2}</math>), subgroup 9, change from "15 ns max" to "17 ns max". Subgroups 10 and 11, change from "18 ns max" to "21 ns max". For output enable time test (<math>t_{PZH1}</math>), subgroups 10 and 11, change from "41 ns max" to "45 ns max". For output enable time test (<math>t_{PZL1}</math>), subgroups 10 and 11, change from "34 ns max" to "37 ns max".  Revision level block; change from "B" to "C".</p> <p>Sheet 6: Table I; for output enable time test (<math>t_{PZH2}</math>), subgroups 10 and 11, change from "50 ns max" to "55 ns max". For output enable time test (<math>t_{PZL2}</math>), subgroups 10 and 11, change from "41 ns max" to "46 ns max". For output disable time test (<math>t_{PHZ2}</math>), subgroups 10 and 11, change from "33 ns max" to "36 ns max". For output disable time test (<math>t_{PLZ2}</math>), subgroups 10 and 11, change from "35 ns max" to "38 ns max". For output enable time test (<math>t_{PZH3}</math>), subgroups 10 and 11, change from "48 ns max" to "53 ns max". For output enable time test (<math>t_{PZL3}</math>), subgroups 10 and 11, change from "43 ns max" to "45 ns max". For output disable time test (<math>t_{PLZ3}</math>), subgroups 10 and 11, change from "27 ns max" to "33 ns max".  Revision level block; change from "B" to "C".</p>			
14. THIS SECTION FOR GOVERNMENT USE ONLY			
a. (X one)	X	(1) Existing document supplemented by the NOR may be used in manufacture.	
		(2) Revised document must be received before manufacturer may incorporate this change.	
		(3) Custodian of master document shall make above revision and furnish revised document.	
b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT  DSCC-VAS		c. TYPED NAME (First, Middle Initial, Last)  Ray Monnin	
d. TITLE  Chief, Team Microelectronics	e. SIGNATURE  Ray Monnin		f. DATE SIGNED (YYMMDD) 96-10-31
15a. ACTIVITY ACCOMPLISHING REVISION  DSCC-VAS	b. REVISION COMPLETED (Signature)  Dan Wonnell		c. DATE SIGNED (YYMMDD) 96-10-31

<b>NOTICE OF REVISION (NOR)</b>		1. DATE (YYMMDD) 96-05-10	Form Approved OMB No. 0704-0188
THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.			
Public reporting burden for this collection is estimated to average 2 hours per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503. PLEASE DO NOT RETURN YOUR COMPLETED FORM TO EITHER OF THESE ADDRESSES. RETURN COMPLETED FORM TO THE GOVERNMENT ISSUING CONTRACTING OFFICER FOR THE CONTRACT/ PROCURING ACTIVITY NUMBER LISTED IN ITEM 2 OF THIS FORM.		2. PROCURING ACTIVITY NO.	
		3. DODAAC	
4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code) Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5765	5. CAGE CODE 67268	6. NOR NO. 5962-R123-96
a. TYPED NAME (First, Middle Initial, Last)		7. CAGE CODE 67268	8. DOCUMENT NO. <b>5962-89681</b>
9. TITLE OF DOCUMENT MICROCIRCUIT, LINEAR, OCTAL GENERAL INTERFACE BUS TRANSCEIVER, MONOLITHIC SILICON		10. REVISION LETTER	
		a. CURRENT A	b. NEW B
11. ECP NO. 89681ECP-01			
12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES All			
13. DESCRIPTION OF REVISION			
<p>Sheet 1: Revisions ltr column; add "B". Revisions description column; add "Changes in accordance with NOR 5962-R123-96". Revisions date column; add "96-05-10". Revision level block; add "B". Rev status of sheets; for sheet 1, 4, 5, and 6 add "B".</p> <p>Sheet 4: Table I: For high level output voltage (terminal) test, <math>V_{OH}</math>, subgroups 1, 2, 3, change subgroup 3 minimum value from "2.7 V" to "2.5 V". For high level output voltage (bus) test, <math>V_{OH}</math>, subgroup 3, change minimum value from "2.2 V" to "2.0 V". For high level output voltage (bus) test, add note "2/". For low level output voltage (bus) test, <math>V_{OL}</math>, add note "2/". Revision level block; add "B".</p> <p>Sheet 5: Table I, Functional test, change footnote in conditions from "2/" to "3/". Revision level block; add "B".</p> <p>Sheet 6: Table I, Footnotes, Change note 2/ to note 3/. Add "2/ May not meet IEEE 488 standard." Revision level block; add "B".</p>			
14. THIS SECTION FOR GOVERNMENT USE ONLY			
a (X one)	X	(1) Existing document supplemented by the NOR may be used in manufacture.	
		(2) Revised document must be received before manufacturer may incorporate this change.	
		(3) Custodian of master document shall make above revision and furnish revised document.	
b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DESC-ELDS		c. TYPED NAME (First, Middle Initial, Last) Michael A. Frye	
d. TITLE Chief, Microelectronics Branch	e. SIGNATURE Michael A. Frye		f. DATE SIGNED (YYMMDD) 96-05-10
15a. ACTIVITY ACCOMPLISHING REVISION DESC-ELDS	b. REVISION COMPLETED (Signature) Sandra Rooney	c. DATE SIGNED (YYMMDD) 96-05-10	

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes to recommended operating conditions and table I. Editorial changes throughout.	95-05-10	M. A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12				

PMIC N/A	PREPARED BY Rick C. Officer	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p>AMSC N/A</p>	CHECKED BY Charles E. Besore			MICROCIRCUIT, LINEAR, OCTAL GENERAL INTERFACE BUS TRANSCEIVER, MONOLITHIC SILICON
	APPROVED BY Michael A. Frye			
	DRAWING APPROVAL DATE 89-08-23	SIZE <b>A</b>	CAGE CODE <b>67268</b>	
	REVISION LEVEL A	SHEET 1 OF 12		

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	55ALS161	Octal general purpose interface bus transceiver

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	flat pack
2	CQCC1-N20	20	square leadless chip carrier

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when Lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage ( $V_{CC}$ )	+7.0 V dc
Input voltage	+5.5 V dc
Low level driver output current	100 mA
Continuous total dissipation $T_A \leq +25^\circ\text{C}$ <sup>1/</sup>	1375 mW
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature ( $T_J$ )	150°C

1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ )	+4.75 V dc min to +5.25 V dc max
Minimum high level input voltage ( $V_{IH}$ ):	
TE and DC, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$	2.0 V dc
Bus and terminal, $T_A = +25^\circ\text{C}$ , $+125^\circ\text{C}$	2.0 V dc
Bus and terminal, $T_A = -55^\circ\text{C}$	2.1 V dc
Maximum low level input voltage ( $V_{IL}$ ):	
TE and DC, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$	0.8 V dc
Bus and terminal, $T_A = -55^\circ\text{C}$ , $+25^\circ\text{C}$	0.8 V dc
Bus and terminal, $T_A = +125^\circ\text{C}$	0.7 V dc
Maximum high level current ( $I_{OH}$ ):	
Bus ports with pull-ups active ( $V_{CC} = 5.0$ V dc)	-5.2 mA
Terminal ports	-800 $\mu\text{A}$
Maximum low level output current ( $I_{OL}$ ):	
Bus ports, $T_A = +25^\circ\text{C}$ , $+125^\circ\text{C}$	48 mA
Bus ports, $T_A = -55^\circ\text{C}$	24 mA
Terminal ports	16 mA
Ambient operating temperature range ( $T_A$ )	-55°C to +125°C

<sup>1/</sup> For operation above  $T_A = +25^\circ\text{C}$ , derate at the rate of 11.0 mW/°C.

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	<b>REVISION LEVEL A</b>	<b>SHEET 2</b>

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.  
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage (terminal)	V <sub>OH</sub> 1	V <sub>CC</sub> = 4.75 V, I <sub>OH</sub> = -800 μA	1, 2, 3	01	2.7		V
High level output voltage (bus)		V <sub>CC</sub> = 4.75 V, I <sub>OH</sub> = -5.2 mA	1, 2		2.5		
			3		2.2		
Low level output voltage (terminal)	V <sub>OL</sub>	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 16 mA,	1, 2, 3	01		0.5	V
Low level output voltage (bus)		V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 48 mA,	1, 2			0.5	
			3			0.55	
Input clamp voltage	V <sub>IC</sub>	V <sub>CC</sub> = 4.75 V, I <sub>I</sub> = -18 mA	1, 2, 3	01		-1.5	V
Bus hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )	V <sub>HYS</sub>	V <sub>CC</sub> = 5 V	1, 3	01	0.4		V
			2		0.25		
Voltage at bus port (driver disabled)	V <sub>I/O</sub> (Bus)	V <sub>CC</sub> = 5 V, I <sub>I(bus)</sub> = 0 mA	1, 2, 3	01	2.5	3.7	V
		V <sub>CC</sub> = 5 V, I <sub>I(bus)</sub> = -12 mA				-1.5	
Current into bus port (power on, driver disabled)	I <sub>I/O</sub> (Bus)	V <sub>CC</sub> = 5 V, V <sub>I(bus)</sub> = -1.5 V to 0.4 V	1, 2, 3	01	-1.3		mA
		V <sub>CC</sub> = 5 V, V <sub>I(bus)</sub> = 0.4 V to 2.5 V			0	-3.2	
		V <sub>CC</sub> = 5 V, V <sub>I(bus)</sub> = 2.5 V to 3.7 V				+2.5	
		V <sub>CC</sub> = 5 V, V <sub>I(bus)</sub> = 3.7 V to 5 V				-3.2	
		V <sub>CC</sub> = 5 V, V <sub>I(bus)</sub> = 5 V to 5.5 V			0	2.5	
		V <sub>CC</sub> = 5 V, V <sub>I(bus)</sub> = 5 V to 5.5 V			0.7	2.5	
Current into bus port (power off)		V <sub>CC</sub> = 0.0 V, V <sub>I(bus)</sub> = 0.0 V to 2.5 V				40	μA
High level input current (terminal, control inputs)	I <sub>IH1</sub>	V <sub>I</sub> = 2.7 V, V <sub>CC</sub> = 5.25 V	1, 2, 3	01		20	μA

See footnotes at end of table.

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		<b>REVISION LEVEL A</b>	<b>SHEET 4</b>

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input current at maximum input voltage (terminal)	I <sub>IH2</sub>	V <sub>I</sub> = 5.5 V, V <sub>CC</sub> = 5.25 V	1, 2, 3	01		100	μA
Low level input current (terminal, control inputs)	I <sub>IL</sub>	V <sub>I</sub> = 0.5 V, V <sub>CC</sub> = 5.25 V	1, 2, 3	01		-100	μA
Low level input current (ATN)		V <sub>I</sub> = 0.5 V, V <sub>CC</sub> = 5.25 V				-200	
Short circuit output current (terminal)	I <sub>OS</sub> 1/	V <sub>CC</sub> = 5.25 V	1, 2, 3	01	-15	-75	mA
Short circuit output current (bus)					-25	-125	
Supply current	I <sub>CC</sub>	V <sub>CC</sub> = 5.25 V, no load, TE and DC Low	1, 2, 3	01		90	mA
Functional tests	FT	See 4.3.1c 2/	7, 8	01			
Propagation delay time, from terminal to bus except SRQ, NDAC and NRFD	t <sub>PLH1</sub>	V <sub>CC</sub> = 4.75 V to 5.25 V, R <sub>1</sub> = R <sub>2</sub> = 500 Ω, C <sub>L</sub> = 50 pF, See figure 3	9	01		17	ns
			10, 11			20	
	t <sub>PHL1</sub>		9		14		
			10, 11		16		
Propagation delay time, from bus to terminal	t <sub>PLH2</sub>	9	01		15	ns	
		10, 11			18		
	t <sub>PHL2</sub>	9		15			
		10, 11		18			
Propagation delay time, from terminal to bus SRQ, NDAC and NRFD	t <sub>PLH3</sub>	9	01		25	ns	
		10, 11			30		
	t <sub>PHL3</sub>	9		14			
		10, 11		16			
Output enable time, from TE to DC to bus ATN, REN, IFC and DAV	t <sub>PZH1</sub>	9	01		30	ns	
		10, 11			41		
	t <sub>PZL1</sub>	9		28			
		10, 11		34			

See footnotes at end of table.

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		REVISION LEVEL A	SHEET 5

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output disable time, from TE or DC to bus ATN, REN, IFC and DAV	t <sub>PHZ1</sub>	V <sub>CC</sub> = 4.75 V to 5.25 V, R <sub>1</sub> = R <sub>2</sub> = 500 Ω, C <sub>L</sub> = 50 pF, See figure 3	9	01		14	ns
			10, 11			16	
	t <sub>PLZ1</sub>		9		19		
			10, 11		24		
Output enable time, from TE or DC to terminal	t <sub>PZH2</sub>	9	01		36	ns	
		10, 11			50		
	t <sub>PZL2</sub>	9		34			
		10, 11		41			
Output disable time, from TE or DC to terminal	t <sub>PHZ2</sub>	9	01		20	ns	
		10, 11			33		
	t <sub>PLZ2</sub>	9		24			
		10, 11		35			
Output enable time, from TE or DC to bus EOI	t <sub>PZH3</sub>	9	01		30	ns	
		10, 11			48		
	t <sub>PZL3</sub>	9		35			
		10, 11		43			
Output disable time, from TE or DC to bus EOI	t <sub>PHZ3</sub>	9	01		19	ns	
		10, 11			25		
	t <sub>PLZ</sub>	9		20			
		10, 11		27			

1/ V<sub>OH</sub> and I<sub>OS</sub> applies for three state outputs only.

2/ Functional test shall be conducted at input test conditions of GND ≤ V<sub>IL</sub> ≤ V<sub>OL</sub> and V<sub>OH</sub> ≤ V<sub>IH</sub> ≤ V<sub>CC</sub>.

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Device type	01
Case outlines	R, S, and 2
Terminal number	Terminal symbol
1	TE
2	REN
3	IFC
4	NDAC
5	NRFD
6	DAV
7	EOI
8	ATN
9	SRQ
10	GND
11	DC
12	SRQ
13	ATN
14	EOI
15	DAV
16	NRFD
17	NDAC
18	IFC
19	REN
20	V <sub>CC</sub>

Pin assignment

Name	Identity class	
DC TE	Direction control Talk enable	Control
ATN SRQ REN IFC EOI	Attention Service request Remote enable Interface clear End or Identity	Bus management
DAV NDAC NRFD	Data valid Not data accepted Not ready for data	Data transfer

Pin identification table

FIGURE 1. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89681</b>
		<b>REVISION LEVEL A</b>	<b>SHEET 7</b>

Controls			Bus-management channels				Data-transfer channels			
DC	TE	ATN*	ATN*	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(Controlled by DC)				(Controlled by TE)			
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

NOTE:

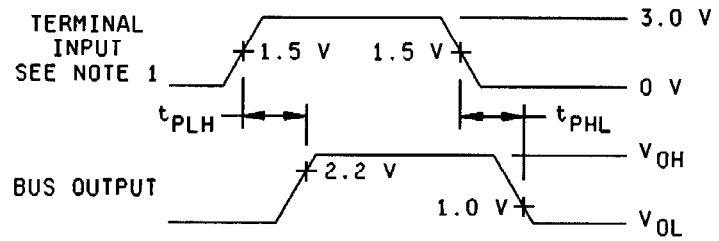
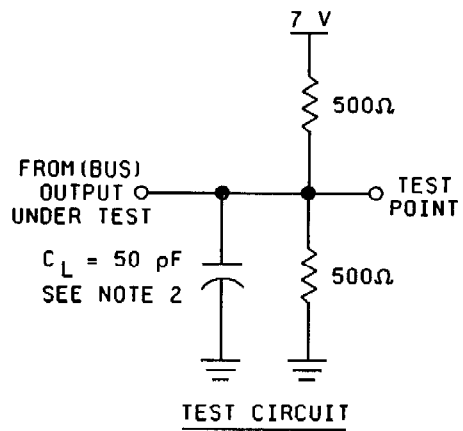
H = High, L = Low, R = Receive, T = Transmit, X = Irrelevant

Direction of data transmission is from the terminal side to the bus side and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

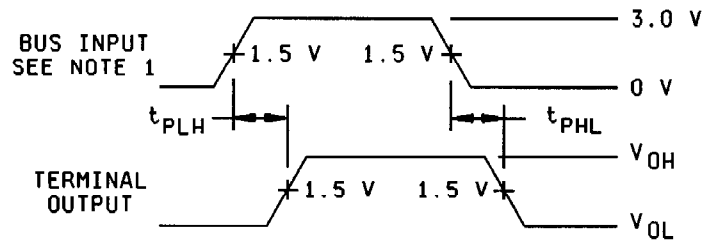
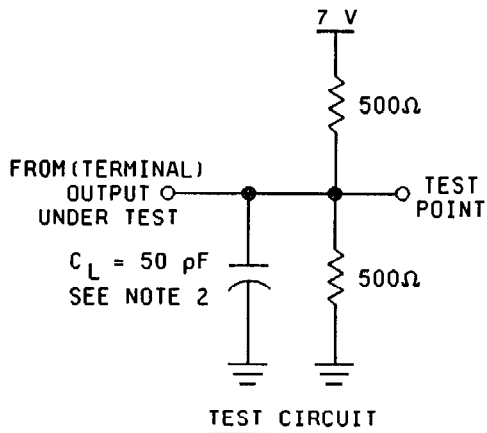
\*ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

FIGURE 2. Truth table.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89681</b>
		<b>REVISION LEVEL A</b>	<b>SHEET 8</b>



TERMINAL-TO-BUS PROPAGATION DELAY TIMES



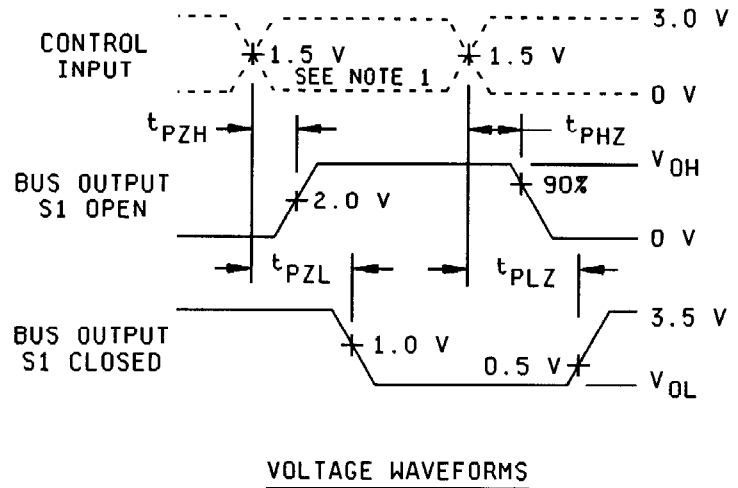
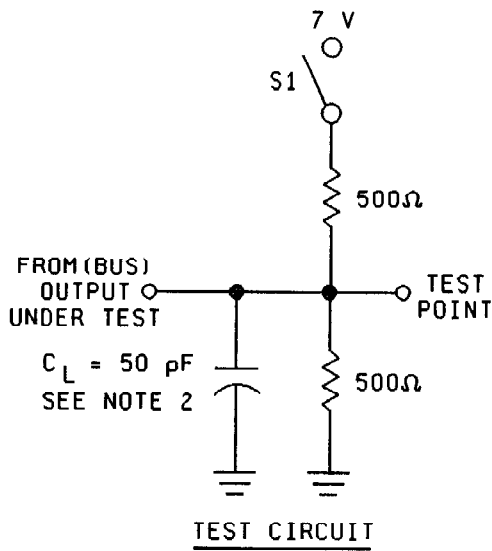
BUS-TO-TERMINAL PROPAGATION DELAY TIMES

NOTES:

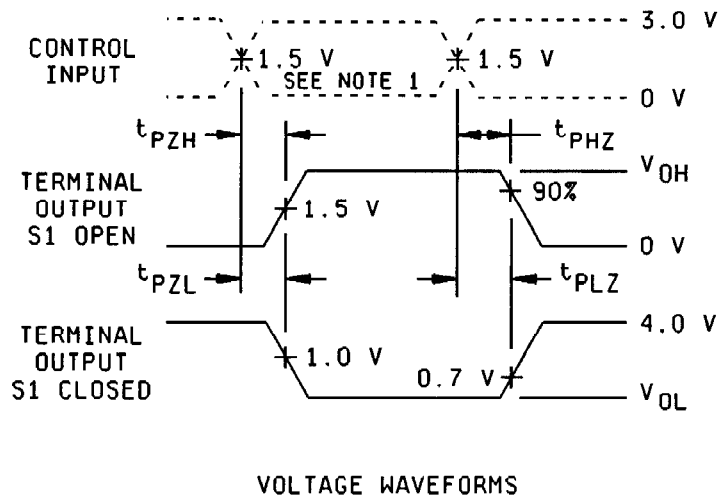
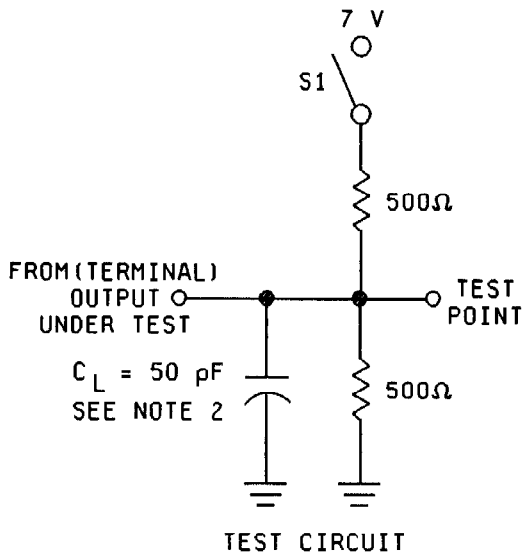
1. The input pulse is supplied by a generator having the following characteristics,  $PRR \leq 1.0 \text{ MHz}$ , 50 percent duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_{out} = 50 \Omega$ .
2.  $C_L$  includes probe and jig capacitance.

FIGURE 3. Test circuits and voltage waveforms.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-89681</b>
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BUS ENABLE AND DISABLE TIMES



TERMINAL ENABLE AND DISABLE TIMES

NOTES:

1. The input pulse is supplied by a generator having the following characteristics, PRR  $\leq$  1.0 MHz, 50 percent duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_{out} = 50 \Omega$ .
2.  $C_L$  includes probe and jig capacitance.

FIGURE 3. Test circuits and voltage waveforms - continued.

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3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

\* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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## STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 95-05-10

Approved sources of supply for SMD 5962-89681 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN <sup>1/</sup>
5962-8968101RX	01295	SNJ55ALS161J
5962-8968101SX	01295	SNJ55ALS161W
5962-89681012X	01295	SNJ55ALS161FK

<sup>1/</sup> Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

01295

Vendor name  
and address

Texas Instruments, Incorporated  
P.O. Box 60448  
Midland, TX 79711-0448

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.