



MICROCIRCUIT DATA SHEET

MNDS1776-X REV 2A0

Original Creation Date: 04/17/96
 Last Update Date: 08/24/98
 Last Major Revision Date: 08/06/98

PI-BUS TRANSCEIVER

General Description

The DS1776 is an octal PI-bus Transceiver. The A to B path is latched. B outputs are open collector with series Schottky diode, ensuring minimum B output loading. B inputs have glitch rejection circuitry, 4 ns typical.

Designed using National's Bi-CMOS process for both low operating and disabled power. AC performance is optimized for the PI-Bus inter-operability requirements.

The DS1776 is an octal latched transceiver and is intended to provide the electrical interface to a high performance wired-or bus. This bus has a loaded characteristic impedance range of 20 Ohm to 50 Ohm and is terminated on each end with a 30 Ohm to 40 Ohm resistor.

The DS1776 is an octal bidirectional transceiver with open collector B and TRI-STATE A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100 mA from 2V and features a controlled linear ramp to minimize crosstalk and ringing on the bus.

A separate high level control voltage (Vx) is provided to prevent the A side output high level from exceeding future high density processor supply voltage levels. For 5V systems, Vx is tied to Vcc.

Industry Part Number

DS1776

NS Part Numbers

DS1776E/883

Prime Die

DS1776

Controlling Document

5962-9231701M3A

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

| Subgrp | Description | Temp (°C) |
|--------|---------------------|-----------|
| 1 | Static tests at | +25 |
| 2 | Static tests at | +125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | +25 |
| 5 | Dynamic tests at | +125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | +25 |
| 8A | Functional tests at | +125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | +25 |
| 10 | Switching tests at | +125 |
| 11 | Switching tests at | -55 |

(Absolute Maximum Ratings)

| | |
|---|---------------------|
| A0-A7 Current Applied to Output in Low Output State (I_o) | 40mA |
| A0-A7, B0-B7 Input Voltage (V_i) | -0.5V to +5.5V |
| B0-B7 Current Applied to Output in Low Output State (I_o) | 200mA |
| ESD Tolerance Czap = 120pF, Rzap = 1500 Ohms | 0.5kV |
| Input Current (I_i) | -40mA to +5mA |
| Lead Temperature (Soldering, 10 seconds) | 260 C |
| Storage Temperature Range | -65 C to +150 C |
| Supply Voltage (V_{cc}) | -0.5V to +7.0V |
| Voltage Applied to Output in High Output State (V_o) | -0.5V to + V_{cc} |
| V_x , V_{oh} Output Level Control Voltage (A Outputs) | -0.5V to +7.0V |
| $\overline{OE}B_n$, $\overline{OE}A$, \overline{LE} Input Voltage (V_i) | -0.5V to +7.0V |
| Power Dissipation LCC PKG | 740 mW |

Recommended Operating Conditions

| | |
|----------------------------------|---------------------|
| Operating Temperature Range (TA) | Min=-55, Max=+125 C |
| Supply Voltage (V_{cc}) | Min=4.5V, Max=5.5V |

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V_{CC} = 5.5V$

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|--------|---|---|-------|----------|-----|------|------|------------|
| Vil2 | Low Level In Voltage B0-B7 | $V_{CC} = 4.5$ | 1 | | | 1.45 | V | 1, 2, 3 |
| Vil1 | All Other Inputs | $V_{CC} = 4.5$ | | | | .8 | V | 1, 2, 3 |
| Vih1 | Hi Level In Voltage OEB0/1, OEA, An, LE | | 1 | | 2 | | V | 1, 2, 3 |
| Vih2 | High Level In Voltage B0-B7 | | | | 1.6 | | V | 1, 2, 3 |
| Ioh1 | High Level Output Current A0-A7 | $V_{CC} = 4.5, V_{in} = V_{ih} \text{ or } V_{il}, V_{oh} = 2.5V$ | 2 | | | -3 | mA | 1, 2, 3 |
| Ioh2 | High Level Output Current B0-B7 | $V_{CC} = 5.5, V_{il} = 0.8V, V_{ih} = 2.0V, V_{oh} = 2.1V$ | | | | 100 | uA | 1, 2, 3 |
| Iol1 | Low Level Output Current A0-A7 | $V_{CC} = 4.5, V_{in} = V_{ih} \text{ or } V_{il}, V_{ol} = 0.5V$ | 3 | | | 20 | mA | 1, 2, 3 |
| Iol2 | Low Level Output Current B0-B7 | $V_{CC} = 4.5, V_{in} = V_{ih} \text{ or } V_{il}, V_{ol} = 1.15V$ | | | | 100 | mA | 1, 2, 3 |
| Voh | High Level Output Voltage A0-A7 | $V_{CC} = 4.5, V_{in} = V_{il} \text{ or } V_{ih}, I_{oh} = -3 \text{ mA}, V_x = 4.5v$ | | | 2.5 | 4.5 | V | 1, 2, 3 |
| | | $V_{CC} = 4.5, V_{in} = V_{il} \text{ or } V_{ih}, I_{oh} = -0.4 \text{ mA}, V_x = 3.13/3.47$ | | | 2.5 | VX | V | 1, 2, 3 |
| Vol | Low Level Output Voltage A0-A7 | $V_{CC} = 4.5, V_{il} = \text{Max}, V_{ih} = \text{Min}, I_{ol} = 20\text{mA}, V_x = V_{CC}$ | | | | 0.5 | V | 1, 2, 3 |
| Volb | Low Level Output Voltage B0-B7 | $V_{CC} = 4.5, V_{il} = \text{Max}, V_{ih} = \text{Min}, I_{ol} = 100\text{mA}$ | | | | 1.15 | V | 1, 2, 3 |
| | | $V_{CC} = 4.5, V_{il} = \text{Max}, V_{ih} = \text{Min}, I_{ol} = 4\text{mA}$ | | | 0.4 | | V | 1, 2, 3 |
| Vik | Input Clamp Voltage A0-A7 | $V_{CC} = 4.5, I_i = -40\text{mA}$ | | | | -0.5 | V | 1, 2, 3 |
| Vik | Input Clamp Voltage Other Inputs | $V_{CC} = 4.5, I_i = -18\text{mA}$ | | | | -1.2 | V | 1, 2, 3 |
| Iih1 | Input Current Max Input Voltage OEBn, OEA, LE | $V_{CC} = 5.5, V_i = 7.0V$ | | | | 100 | uA | 1, 2, 3 |
| Iih2 | Input Current Max Input Voltage A0-A7, B0-B7 | $V_{CC} = 5.5, V_i = 5.5V$ | | | | 1 | mA | 1, 2, 3 |
| Iih3 | High Level Input Current OEBn, OEA, LE | $V_{CC} = 5.5, V_i = 2.7V$ | | | | 20 | uA | 1, 2, 3 |

Electrical Characteristics

DC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V_{CC} = 5.5V$

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|------------|--|--|-------|----------|------|------|------|------------|
| Iih4 | High Level Input Current B0-B7 | $V_{CC} = 5.5, V_i = 2.1V$ | | | | 100 | uA | 1, 2, 3 |
| Iil1 | Low Level Input Current OEBn, OEA | $V_{CC} = 5.5, V_i = 0.5V$ | | | | -20 | uA | 1, 2, 3 |
| Iil2 | Low Level Input Current LE | $V_{CC} = 5.5, V_i = 0.5V$ | | | | -20 | uA | 1 |
| | | | | | | -40 | uA | 2, 3 |
| Iil3 | Low Level Input Current B0-B7 | $V_{CC} = 5.5, V_i = 0.3V$ | | | | -100 | uA | 1, 2, 3 |
| Iozh + Iih | TRI-STATE Output Current, High Level Voltage Applied A0-A7 | $V_{CC} = 5.5, V_o = 2.7V$ | | | | 70 | uA | 1, 2, 3 |
| Iozl + Iil | TRI-STATE Output Current, Low Level Voltage Applied A0-A7 | $V_{CC} = 5.5, V_o = 0.5V$ | | | | -70 | uA | 1, 2, 3 |
| Ix | High Level Control Current | $V_{CC}=5.5, V_x=5.5V, \overline{LE}=OEA=\overline{OEBn}=2.7V, A0-A7 = 2.7, B0-B7 = 2V$ | | | -100 | 100 | uA | 1, 2, 3 |
| | | $V_{CC}=5.5, V_x=3.13V \text{ and } 3.47V, \overline{LE}=OEA=2.7V, \overline{OEBn}=A0-A7=2.7V, B0-B7=2V$ | | | -10 | 10 | mA | 1, 2, 3 |
| Ios | Short Circuit Output Current A0-A7 only | $V_{CC}=5.5, B_n = 1.9V, OEA = 2.0V, \overline{OEBn} = 2.7V, V_{out} = 0V$ | 4 | | -60 | -150 | mA | 1, 2, 3 |
| Icch | Supply Current (Total) ICCH | $V_{CC}=5.5, V_{in} (A_n) = 5.0V$ | | | | 37 | mA | 1, 2 |
| | | | | | | 41 | mA | 3 |
| Iccl | Supply Current (Total) ICCL | $V_{CC}=5.5, V_{in} (A_n) = 0.5V$ | | | | 38 | mA | 1, 3 |
| | | | | | | 34 | mA | 2 |
| Iccz | Supply Current (Total) ICCZ | $V_{CC}=5.5, V_{in} (A_n) = 0.5V$ | | | | 35 | mA | 1, 2, 3 |
| Ioff | Power Off Output Current B0-B7 | $V_{CC}=0, B_n = 2.1V, V_{il} = \text{Max}, V_{ih} = \text{Min}$ | | | | 100 | uA | 1, 2, 3 |

Electrical Characteristics

AC PARAMETERS: B to A PATH

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $V_{cc} = 5V \pm 10\%$, $C_1 = 50pF$, $R_1 = 500 \text{ Ohms}$

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|--------|-----------------------------|------------|-------|----------|-----|-----|------|--------------|
| TPLH | Propagation Delay B to A | | | | 4.5 | 17 | nS | 9, 10, 11 |
| TPHL | Propagation Delay B to A | | | | 6.0 | 17 | nS | 9, 10, 11 |
| TPZH | Output Enable OEA To A | | | | 4.0 | 17 | nS | 9, 10, 11 |
| TPZL | Output Enable OEA To A | | | | 4.0 | 21 | nS | 9, 10, 11 |
| TPHZ | Output Disable OEA to A | | | | 2.0 | 12 | nS | 9, 10, 11 |
| TPLZ | Output Disable OEA to A | | | | 2.0 | 13 | nS | 9, 10, 11 |

AC PARAMETERS: A to B PATH

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $V_{cc} = 5V \pm 10\%$, $C_1 = 30pF$, $R_1 = 9 \text{ Ohms}$

| | | | | | | | | |
|------|----------------------------------|--|--|--|-----|----|----|--------------|
| TPLH | Propagation Delay A to B | | | | 2.0 | 13 | nS | 9, 11 |
| | | | | | | | | |
| TPHL | Propagation Delay A to B | | | | 2.5 | 13 | nS | 9, 10, 11 |
| TPLH | Propagation Delay LE to B | | | | 2.0 | 16 | nS | 9, 11 |
| TPLH | Propagation Delay LE to B | | | | 2.0 | 22 | nS | 10 |
| TPHL | Propagation Delay LE to B | | | | 2.0 | 16 | nS | 9, 10, 11 |
| TPLH | Enable/Disable Time OEBn to B | | | | 2.0 | 13 | nS | 9, 11 |
| TPLH | Enable/Disable Time OEBn to B | | | | 2.0 | 16 | nS | 10 |
| TPHL | Enable/Disable Time OEBn to B | | | | 3.5 | 14 | nS | 9 |
| TPHL | Enable/Disable Time OEBn to B | | | | 3.5 | 13 | nS | 10 |
| TPHL | Enable/Disable Time OEBn to B | | | | 3.5 | 16 | nS | 11 |

Electrical Characteristics

AC PARAMETERS: SETUP/HOLD/PULSE WIDTH SPECS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: $V_{cc} = 5V \pm 10\%$

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|--------|--------------------|------------|-------|----------|-----|-----|------|------------|
| TS | A to LE Setup | | | | 7.0 | | nS | 9, 10, 11 |
| TH | A to LE Hold | | | | 0.0 | | nS | 9, 10, 11 |
| TW | LE Pulse Width Low | | | | 12 | | nS | 9, 10, 11 |

Note 1: Tested Go/No Go.

Note 2: Same as Voh.

Note 3: Same as Vol.

Note 4: Not more than one output to be shorted at a time.

Graphics and Diagrams

| GRAPHICS# | DESCRIPTION |
|-----------|---|
| 6138HRC1 | 28L LEADLESS CHIP CARRIER TYPE C(B/I CKT) |
| E28ARD | LCC (E), TYPE C, 28 TERMINAL(P/P DWG) |

See attached graphics following this page.

Revision History

| Rev | ECN # | Rel Date | Originator | Changes |
|------------|--------------|-----------------|-------------------|---|
| 2A0 | M0003000 | 08/24/98 | Mike Fitzgerald | Changed tpZL (Output Enable OEA to A) maximum limit from 17ns to 21ns, subgroups 9,10,11. |