MOTOROLA

Military 54LS366A

Hex Inverter, Common Enable, 3-State Outputs

ELECTRICALLY TESTED PER: MIL-M-38510/32202

This device is a high-speed hex buffer with 3-state outputs. It is organized as a single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable (E) is LOW.

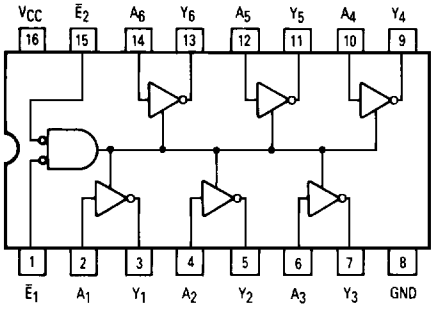
When the Output Enable (E) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

AVAILABLE AS:

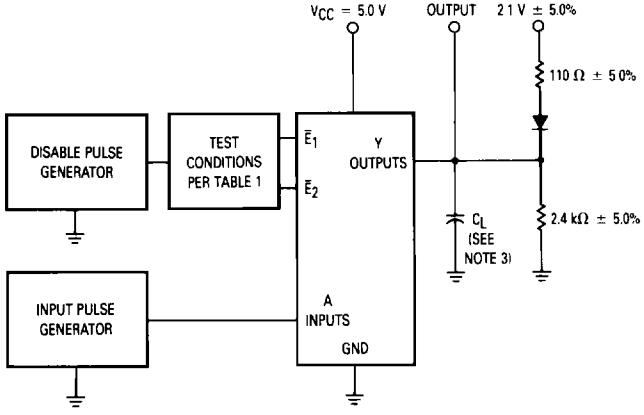
1) JAN: JM38510/32202BXA
2) SMD: *
3) 883C: 54LS366A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2
***Call Factory for latest update**

LOGIC DIAGRAM



AC TEST CIRCUIT



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\bar{E}_1$	1	1	2	GND
A_1	2	2	3	GND
Y_1	3	3	4	V_{CC}
A_2	4	4	5	GND
Y_2	5	5	7	V_{CC}
A_3	6	6	8	GND
Y_3	7	7	9	V_{CC}
GND	8	8	10	GND
Y_4	9	9	12	V_{CC}
A_4	10	10	13	GND
Y_5	11	11	14	V_{CC}
A_5	12	12	15	GND
Y_6	13	13	17	V_{CC}
A_6	14	14	18	GND
$\bar{E}_2$	15	15	19	GND
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Inputs			Output
$\bar{E}_1$	$\bar{E}_2$	D	
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)

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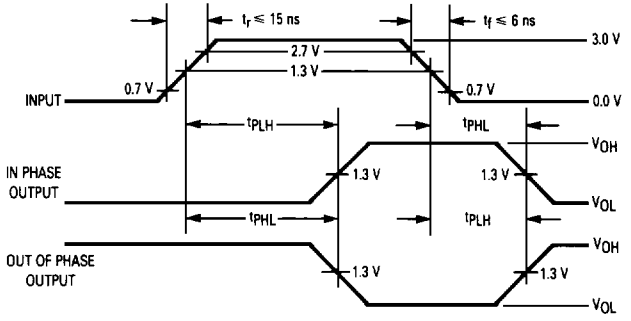
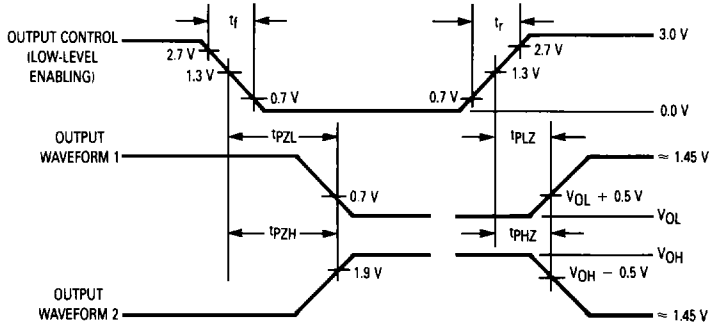
WAVEFORMS



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times, Three-State Outputs

NOTES:
1. Pulse generator has the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).
3. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance.
4. Voltage measurements are to be made with respect to network ground terminal.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IL} = 0.7 V, $\overline{E}_n$ = 0.7 V, other inputs are open.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, V_{IH} = 2.0 V, $\overline{E}_n$ = 0.7 V, other inputs are open.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IL}	Logical "0" Input Current	−160	−400	−160	−400	−160	−400	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, $\overline{E}_n$ = 0.4 V, other inputs are open.
$I_{IL(E_n)}$	Logical "0" Input Current	−160	−400	−160	−400	−160	−400	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V (E_n), other inputs are open.
I_{OS}	Output Short Circuit Current	−30	−130	−30	−130	−30	−130	mA	V_{CC} = 5.5 V, V_{OUT} = GND, $\overline{E}_n$ = 0.7 V, other inputs are open.
I_{OZH}	Output Off Current High		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.0 V, $\overline{E}_n$ = 2.0 V or 0.7 V, V_{IL} = 0.7 V, V_{OUT} = 2.4 V, other inputs are open.
I_{OZL}	Output Off Current Low		−20		−20		−20	μA	V_{CC} = 5.5 V, V_{IL} = 0.7 V, $\overline{E}_n$ = 2.0 V or 0.7 V, V_{IH} = 2.0 V, V_{OUT} = 0.4 V, other inputs are open.
I_{CC}	Power Supply Current		21		21		21	mA	V_{CC} = 5.5 V, V_{IN} = GND, $\overline{E}_n$ = 4.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V. V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL} t_{PHL}	Propagation Delay /Data-Output Output High-Low	2.0	18 18	2.0	23 23	2.0	23 23	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω ± 5.0%. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLH} t_{PLH}	Propagation Delay /Data-Output Output Low-High	2.0	15 15	2.0	20 19	2.0	20 19	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω ± 5.0%. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZH} t_{PZH}	Propagation Delay /Data-Output Output High-Low	2.0	35 35	2.0	45 44	2.0	45 44	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω ± 5.0%. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZL} t_{PZL}	Propagation Delay /Data-Output Output Low-High	2.0	45 45	2.0	58 56	2.0	58 56	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω ± 5.0%. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PHZ} t_{PHZ}	Propagation Delay /Data-Output Output High-Low	2.0	32 32	2.0	42 40	2.0	42 40	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω ± 5.0%. V_{CC} = 5.0 V, C_L = 5.0 pF, R_L = 667 Ω.
t_{PLZ} t_{PLZ}	Propagation Delay /Data-Output Output Low-High	2.0	35 35	2.0	45 44	2.0	45 44	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω ± 5.0%. V_{CC} = 5.0 V, C_L = 5.0 pF, R_L = 667 Ω.

NOTE:
1. The limits specified for C_L = 45 pF and C_L = 5.0 pF are guaranteed but not tested.