National Semiconductor

November 1998

# LM4540
# AC '97 Codec with National 3D Sound

## General Description

The LM4540 is an audio codec for PC systems which performs the analog-intensive function of the Analog Codec '97 Rev 1.03 architecture. Using 18-Bit ΣΔ A/D and D/A converters, the LM4540 provides 90dB of dynamic range.

The LM4540 was designed specifically to provide a high quality audio path and provide all analog functionality in a PC audio system. It features full duplex stereo A/D's and D/A's and an analog mixer with 2 stereo and 3 mono inputs, each of which has separate gain, attenuation and mute control. In addition, the LM4540 provides National's 3D Sound stereo enhancement technology.

The LM4540 features AC-Link, a synchronous, fixed rate serial bus for connection to the digital AC '97 Controller. The separation of the analog and digital functions of the AC '97 architecture allows for system design flexibility and increased overall performance.

## Key Specifications

- Analog Mixer Dynamic Range 95dB (typ)
- D/A Dynamic Range 89dB (typ)
- A/D Dynamic Range 90dB (typ)

## Features

- Audio Codec '97 compliant
- Stereo 18-Bit ΣΔ A/D's and D/A's with 128X oversampling
- National's 3D Sound circuitry
- Power management support
- Digital Interface 3V and 5V compliant

## Applications

- PC Audio Systems Requiring Only 2 Stereo Inputs (CD, Line) and 3 Mono Inputs (Mic, Phone, PC Beep)

## Block Diagram

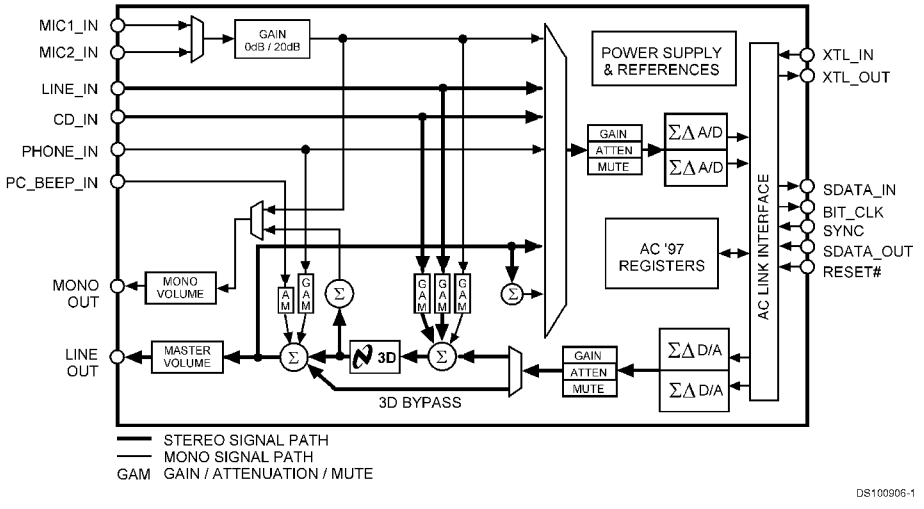



**FIGURE 1. LM4540 Block Diagram**

## Absolute Maximum Ratings (Note 3)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 6.0V |
| Storage Temperature | −65˚C to +150˚C |
| Input Voltage | −0.3V to $V_{DD}$ +0.3V |
| ESD Susceptibility (Note 5) | 2500V |
| pins 27, 28 | 1500V |
| pin 3 | 750V |
| ESD Susceptibility (Note 6) | 200V |
| pin 3 | 100V |
| Junction Temperature | 150˚C |
| Soldering Information | |
| TQFP Package | |
| Vapor Phase (60 sec.) | 215˚C |
| Infrared (15 sec.) | 220˚C |

See AN-450 "Surface Mounting and their Effects on Product Reliability" for other methods of soldering surface mount devices.

$\theta_{JA}$ (typ)— VBH48A 74˚C/W

## Operating Ratings

| | |
|---|---|
| Temperature Range | |
| $T_{MIN} \le T_A \le T_{MAX}$ | $-40˚C \le T_A \le 85˚C$ |
| Analog Supply Range | $4.2V \le AV_{DD} \le 5.5V$ |
| Digital Supply Range | $3.0V \le DV_{DD} \le 5.5V$ |

## Electrical Characteristics (Notes 1, 3)

The following specifications apply for $AV_{DD}$ = 5V, $DV_{DD}$ = 5V unless otherwise noted. Limits apply for $T_A$= 25˚C. The reference for 0dB is 1Vrms unless otherwise specified.

| Symbol | Parameter | Conditions | LM4540 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (Note 7) | Limit (Note 8) | |
| $AV_{DD}$ | Analog Supply Range | | | 4.2 | V (min) |
| | | | | 5.5 | V (max) |
| $DV_{DD}$ | Digital Supply Range | | | 3.0 | V (min) |
| | | | | 5.5 | V (max) |
| $I_{DDD}$ | Digital Quiescent Power Supply Current | $D_{VDD}$ = 5V | 38 | | mA |
| | | $D_{VDD}$ = 3.3V | 20 | | mA |
| $I_{DDA}$ | Analog Quiescent Power Supply Current | | 55 | | mA |
| $I_{SD}$ | Shutdown Current | | 1.5 | | mA |
| $V_{REF}$ | Reference Voltage | | 2.23 | | V |
| PSRR | Power Supply Rejection Ratio | | 40 | | dB |
| **Analog Loopthru Mode** | | | | | |
| | Dynamic Range (Note 2) | CD Input to Line Output, -60dB Input THD+N, A-Weighted | 95 | 90 | dB (min) |
| THD | Total Harmonic Distortion | $V_O$ = -3dB, f = 1kHz, $R_L$ = 10kΩ | 0.01 | 0.02 | % (max) |
| **Analog Input Section** | | | | | |
| $V_{IN}$ | Line Input Voltage | | 1 | | Vrms |
| | Mic Input with 20dB Gain | | 0.1 | | Vrms |
| | Mic Input with 0dB Gain | | 1 | | Vrms |
| Xtalk | Crosstalk | CD Left to Right | -85 | -70 | dB (max) |
| $Z_{IN}$ | Input Impedance | | 40 | 10 | kΩ (min) |
| $C_{IN}$ | Input Capacitance | | 15 | | pF |
| | Interchannel Gain Mismatch | CD Left to Right | 0.04 | | dB |
| **Record Gain Amplifier - A/D** | | | | | |
| $A_S$ | Step Size | 0dB to 22.5dB | 1.5 | | dB |
| **Mixer Section** | | | | | |
| $A_S$ | Step Size | +12dB to -34.5dB | 1.5 | | dB |
| $A_M$ | Mute Attenuation | | 86 | | dB |
| **Analog to Digital Converters** | | | | | |
| | Resolution | | 18 | | Bits |

## Electrical Characteristics (Notes 1, 3) (Continued)

The following specifications apply for $AV_{DD}$ = 5V, $DV_{DD}$ = 5V unless otherwise noted. Limits apply for $T_A$= 25˚C. The reference for 0dB is 1Vrms unless otherwise specified.

| Symbol | Parameter | Conditions | LM4540 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (Note 7) | Limit (Note 8) | |
| **Analog to Digital Converters** | | | | | |
| | Dynamic Range (Note 2) | -60dB Input THD+N, A-Weighted | 90 | 75 | dB (min) |
| | Frequency Response | -1dB Bandwidth | 20 | | kHz |
| **Digital to Analog Converters** | | | | | |
| | Resolution | | 18 | | Bits |
| | Dynamic Range (Note 2) | -60dB Input THD+N, A-Weighted | 89 | 85 | dB (min) |
| THD | Total Harmonic Distortion | $V_{IN}$ = -3dB, f=1kHz, $R_L$ = 10kΩ | 0.01 | 0.03 | % (max) |
| | Frequency Response | -1dB Bandwidth | 21 | | kHz |
| | Group Delay (Note 2) | | | 1 | mS (max) |
| | Out of Band Energy | | -40 | | dB |
| | Stop Band Rejection | | 70 | | dB |
| $D_T$ | Discrete Tones | | -96 | | dB |
| **Output Volume Section** | | | | | |
| $A_S$ | Step Size | 0dB to -46.5dB | 1.5 | | dB |
| $A_M$ | Mute Attenuation | | 86 | | dB |
| **Digital I/O** (Note 2) | | | | | |
| $V_{IL}$ | Low level input voltage | | | 0.30 x DVDD | V (max) |
| $V_{HI}$ | High level input voltage | | | 0.40 x DVDD | V (min) |
| $V_{OH}$ | High level output voltage | | | 0.50 x DVDD | V (min) |
| $V_{OL}$ | Low level output voltage | | | 0.20 x DVDD | V (max) |
| $I_L$ | Input Leakage Current | AC Link inputs | | ±10 | µA (max) |
| $I_L$ | Tri state Leakage Current | High impedance AC Link outputs | | ±10 | µA (max) |
| $I_{DR}$ | Output drive current | AC Link outputs | 5 | | mA |
| **Digital Timing Specifications** (Note 2) | | | | | |
| $F_{BC}$ | BIT_CLK frequency | | 12.288 | | MHz |
| $T_{BCP}$ | BIT_CLK period | | 81.4 | | nS |
| $T_{CH}$ | BIT_CLK high | Variation of BIT_CLK period from 50% duty cycle | | ±20 | % (max) |
| $F_{SYNC}$ | SYNC frequency | | 48 | | kHz |
| $T_{SP}$ | SYNC period | | 20.8 | | µS |
| $T_{SH}$ | SYNC high pulse width | | 1.3 | | µS |
| $T_{SL}$ | SYNC low pulse width | | 19.5 | | µS |
| $T_{SETUP}$ | Setup Time | SDATA_IN, SDATA_OUT to falling edge of BIT_CLK | | 15 | nS (min) |
| $T_{HOLD}$ | Hold Time | Hold time of SDATA_IN, SDATA_OUT from falling edge of BIT_CLK | | 5 | nS (min) |
| $T_{RISE}$ | Rise Time | BIT_CLK, SYNC, SDATA_IN or SDATA_OUT | | 6 | nS (max) |
| $T_{FALL}$ | Fall Time | BIT_CLK, SYNC, SDATA_IN or SDATA_OUT | | 6 | nS (max) |
| $T_{RST\_LOW}$ | RESET# active low pulse width | For cold reset | | 1.0 | µS (min) |
| $T_{RST2CLK}$ | RESET# inactive to BIT_CLK start up | For cold reset | | 162.8 | nS (min) |

## Electrical Characteristics (Notes 1, 3) (Continued)

The following specifications apply for $AV_{DD}$ = 5V, $DV_{DD}$ = 5V unless otherwise noted. Limits apply for $T_A$= 25˚C. The reference for 0dB is 1Vrms unless otherwise specified.

| Symbol | Parameter | Conditions | LM4540 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (Note 7) | Limit (Note 8) | |
| **Digital Timing Specifications** (Note 2) | | | | | |
| $T_{SH}$ | SYNC active high pulse width | For warm reset | 1.3 | | µS |
| $T_{SYNC2CLK}$ | SYNC inactive to BIT_CLK start up | For warm reset | | 162.8 | nS (min) |
| $T_{SU2RST}$ | Setup to trailing edge of RESET# | For ATE Test Mode | | 15 | nS (min) |
| $T_{RST2HZ}$ | Rising edge of RESET# to Hi-Z | For ATE Test Mode | | 25 | nS (max) |

**Note 1:** All voltages are measured with respect to the ground pin, unless otherwise specified.

**Note 2:** These specifications are guaranteed by design and characterization; they are not production tested.

**Note 3:** *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

**Note 4:** The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4540, $T_{JMAX}$ = 150˚C. The typical junction-to-ambient thermal resistance is 74˚C/W for package number VBH48A.

**Note 5:** Human body model, 100 pF discharged through a 1.5 kΩ resistor.

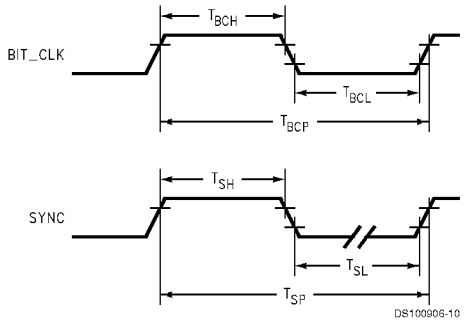
**Note 6:** Machine Model, 220 pF–240 pF discharged through all pins.

**Note 7:** Typicals are measured at 25˚C and represent the parametric norm.

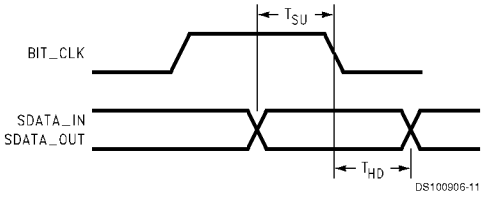
**Note 8:** Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

## Timing Diagrams

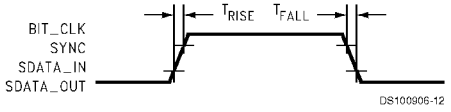
**Clocks**



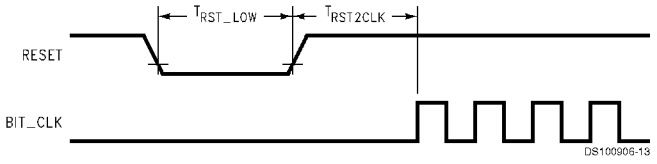

**Data Setup and Hold**



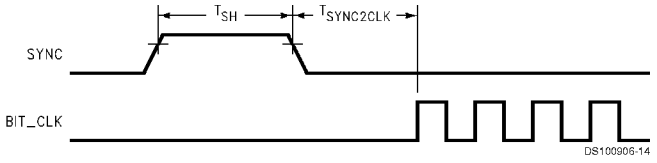

**Digital Rise and Fall**




**Cold Reset**




**Warm Reset**



## Typical Application

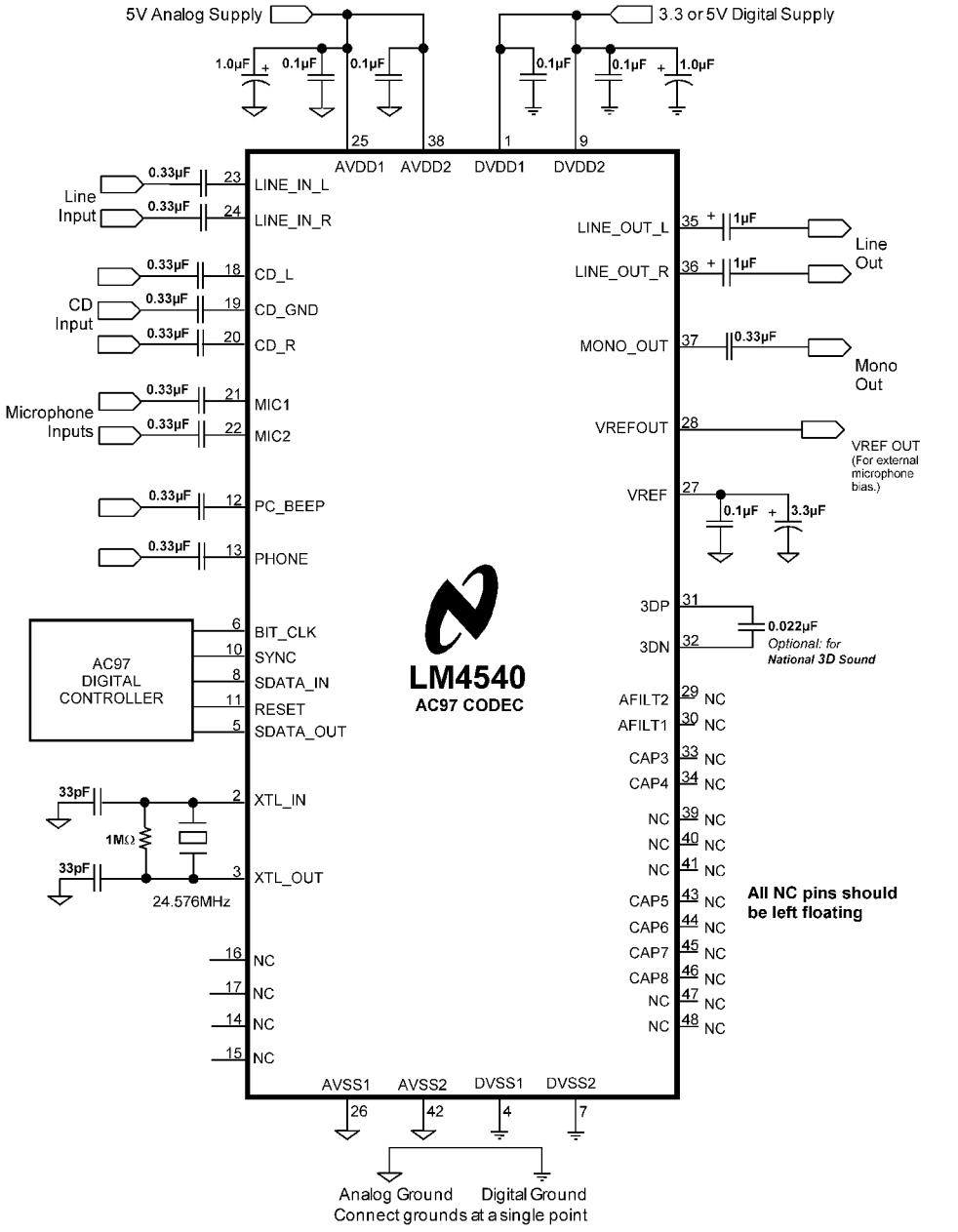
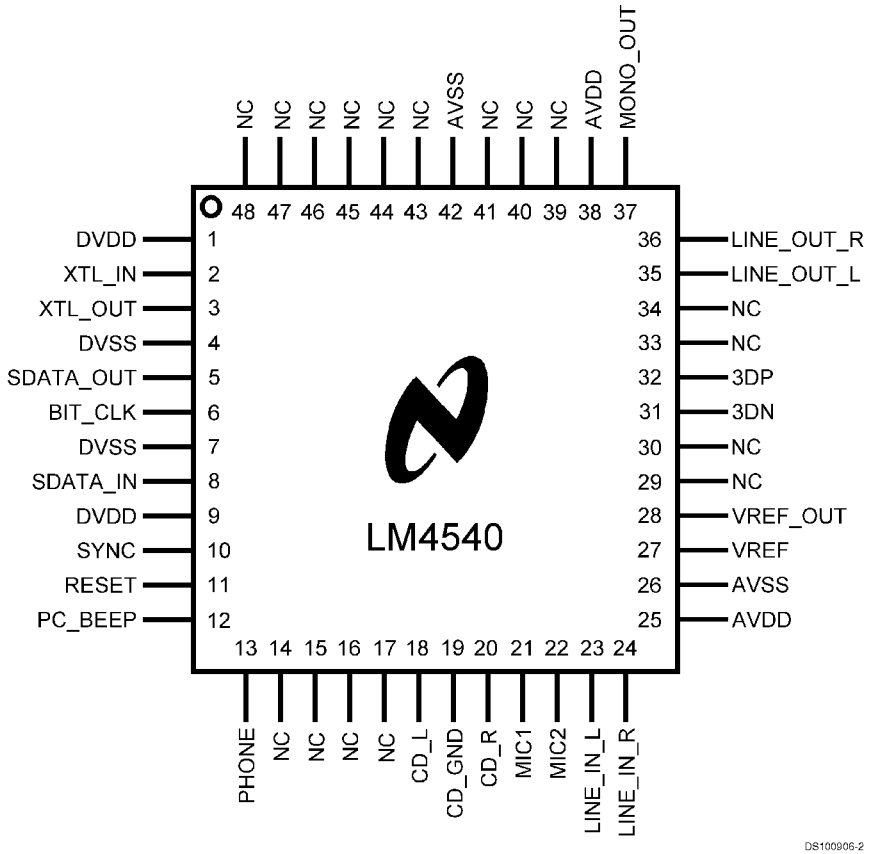



**FIGURE 2. LM4540 Typical Application Circuit**

## Connection Diagram




**Top View**
**Order Number LM4540VH**
**See NS Package Number VBH48A**

## Pin Description

### Analog I/O

| Name | Pin | I / O | Functional Description |
|---|---|---|---|
| PC_BEEP | 12 | I | This is a mono input which gets summed into the stereo line output after the National 3D Sound block. The PC_BEEP level can be adjusted from 0dB to −45dB in 3dB steps, or muted, via register 0Ah. |
| PHONE | 13 | I | This is a mono input which gets summed into the stereo line output after the National 3D Sound block. The PHONE level can be adjusted from +12dB to −34.5dB in 1.5dB steps as well as muted via register 0Ch. |
| CD_L | 18 | I | This line level input can be routed through the Input Mux and recorded by the left ADC. In addition, this analog input gets summed into the left output stream. The amount of CD_L signal mixed in the left output stream can be adjusted from +12dB to −34.5dB in 1.5dB steps as well as muted via register 12h. |
| CD_GND | 19 | I | This input can be used to reject common mode signals on the CD_L or CD_R inputs. CD_GND is an AC ground point not a DC ground point. This input must be AC-coupled to the CD input signal's ground. |

## Pin Description (Continued)

## Analog I/O (Continued)

| Name | Pin | I / O | Functional Description |
|---|---|---|---|
| CD_R | 20 | I | This line level input can be routed through the Input Mux and recorded by the right ADC. In addition, this analog input gets summed into the right output stream. The amount of CD_R signal mixed in the right output stream can be adjusted from +12dB to –34.5dB in 1.5dB steps as well as muted via register 12h. |
| MIC1 | 21 | I | Either MIC1 or MIC2 can be selected via software and routed through the Input Mux for recording. The 20dB boost circuit is enabled/disabled via register 0Eh. Also, the amount of mic signal mixed in the output stream can be adjusted from +12dB to –34.5dB in 1.5dB steps as well as muted via register 0Eh. |
| MIC2 | 22 | I | Either MIC1 or MIC2 can be selected via software and routed through the Input Mux for recording. The 20dB boost circuit is enabled/disabled via register 0Eh. Also, the amount of mic signal mixed in the output stream can be adjusted from +12dB to –34.5dB in 1.5dB steps as well as muted via register 0Eh. |
| LINE_IN_L | 23 | I | This line level input can be routed through the Input Mux and recorded by the left ADC. In addition, this analog input gets summed into the left output stream. The amount of LINE_IN_L signal mixed in the left output stream can be adjusted from +12dB to –34.5dB in 1.5dB steps as well as muted via register 10h. |
| LINE_IN_R | 24 | I | This line level input can be routed through the Input Mux and recorded by the right ADC. In addition, this analog input gets summed into the right output stream. The amount of LINE_IN_R signal mixed in the right output stream can be adjusted from +12dB to –34.5dB in 1.5dB steps as well as muted via register 10h. |
| LINE_OUT_L | 35 | O | This is a post-mixed output for the left audio channel. The level of this output can be adjusted from 0dB to –45dB in 1.5dB steps as well as muted via register 02h. |
| LINE_OUT_R | 36 | O | This is a post-mixed output for the right audio channel. The level of this output can be adjusted from 0dB to –45dB in 1.5dB steps as well as muted via register 02h. |
| MONO_OUT | 37 | O | This line level output can be switched between outputting the post-mixed combined left and right outputs or the mic signal. The level of this output can be adjusted from 0dB to –45dB in 1.5dB steps as well as muted via register 06h. |

## Pin Description (Continued)

## Digital I/O and Clocking

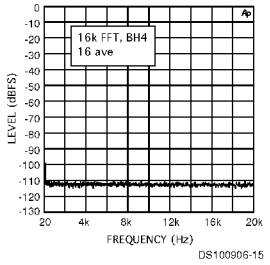
| Name | Pin | I / O | Functional Description |
|---|---|---|---|
| XTL_IN | 2 | I | 24.576 MHz crystal input. Use a fundamental-mode type crystal. When operating from a crystal, a 1MΩ resistor must be connected across pins 2 and 3. |
| XTL_OUT | 3 | O | 24.576 MHz crystal output. When operating from a crystal, a 1MΩ resistor must be connected across pins 2 and 3. |
| SDATA_OUT | 5 | I | This data stream contains both control data and DAC audio data. This input is sampled by the LM4540 on the falling edge of BIT_CLK. |
| BIT_CLK | 6 | O | 12.288 MHz clock which is derived (divide by two) from the 24.576MHz crystal input (XTL_IN). |
| SDATA_IN | 8 | O | This data stream contains both status data and ADC audio data. This output is clocked out by the LM4540 on the rising edge of BIT_CLK. |
| SYNC | 10 | I | 48kHz sync pulse which signifies the beginning of both the SDATA_IN and SDATA_OUT serial streams. SYNC must be synchronous to BIT_CLK. |
| RESET# | 11 | I | This active low signal causes a hardware reset which returns the control registers to their default conditions. |

## Power Supplies and References

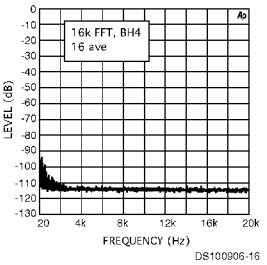
| Name | Pin | I / O | Functional Description |
|---|---|---|---|
| AVDD | 25,38 | I | Analog supply pins. |
| AVSS | 26,42 | I | Analog ground pins. |
| DVDD | 1,9 | I | Digital supply pins. |
| DVSS | 4,8 | I | Digital ground pins. |
| VREF | 27 | O | Nominal 2.2V reference output. Not intended to sink or source current. Bypassing of this pin should be done with short traces to maximize performance. |
| VREFOUT | 28 | O | Nominal 2.2V reference output. Can source up to 5mA of current and can be used to bias a microphone. Do not connect any external capacitance to this pin. |
| AFILT1 | 29 | O | This pin is not used and should be left open (NC). However, a capacitor to ground on this pin is permitted as it will not affect performance. |
| AFILT2 | 30 | O | This pin is not used and should be left open (NC). However, a capacitor to ground on this pin is permitted as it will not affect performance. |
| 3DP,3DN | 31,32 | O | These pins are used to complete the National 3D Sound circuit. Connect a 0.022µF capacitor between pins 3DP and 3DN. The National 3D Sound can be turned on and off via control register 20h. This is a fixed-depth type stereo enhance circuit, thus writing to register 22h has no effect. If National 3D Sound is not desired, then these pins should be left as no connect (NC). |

# Typical Performance Characteristics

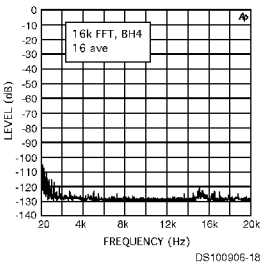
**ADC Noise Floor**



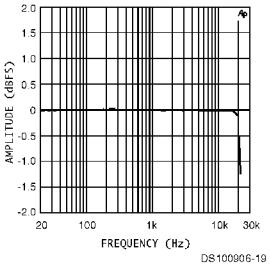

**DAC Noise Floor**



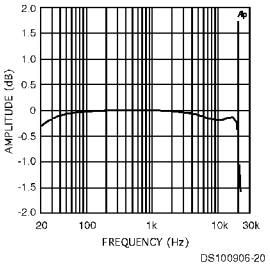

**Analog Loopthru Noise Floor**




**ADC Frequency Response**




**DAC Frequency Response**



## Register Map

| REG | Name | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | Reset | X | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0d50h |
| 02h | Master Volume | Mute | X | X | ML4 | ML3 | ML2 | ML1 | ML0 | X | X | X | MR4 | MR3 | MR2 | MR1 | MR0 | 8008h |
| 06h | Master Volume Mono | Mute | X | X | X | X | X | X | X | X | X | X | MM4 | MM3 | MM2 | MM1 | MM0 | 8000h |
| 08h | Reserved | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 0Ah | PC_BEEP Volume | Mute | X | X | X | X | X | X | X | X | X | X | PV3 | PV2 | PV1 | PV0 | X | 8008h |
| 0Ch | Phone Volume | Mute | X | X | X | X | X | X | X | X | X | X | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h |
| 0Eh | Mic Volume | Mute | X | X | X | X | X | X | X | X | 20dB | X | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h |
| 10h | Line In Volume | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 12h | CD Volume | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 18h | PCM Out Vol | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 1Ah | Record Select | X | X | X | X | X | SL2 | SL1 | SL0 | X | X | X | X | X | SR2 | SR1 | SR0 | 0000h |
| 1Ch | Record Gain | Mute | X | X | X | GL3 | GL2 | GL1 | GL0 | X | X | X | X | GR3 | GR2 | GR1 | GR0 | 8000h |
| 1Eh | Reserved | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 20h | General Purpose | POP | X | 3D | X | X | X | MIX | MS | LPBK | X | X | X | X | X | X | X | 0000h |
| 22h | 3D Control (3D has fixed center and depth) | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 24h | Reserved | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 26h | Powerdown Ctrl/Stat | X | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 | X | X | X | X | REF | ANL | DAC | ADC | na |
| 28h | Reserved | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 5Ah | Vendor Reserved | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 7Ah | Vendor Reserved | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| 7Ch | Vendor ID1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 4E53h |
| 7Eh | Vendor ID2 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4300h |

# Application Information

### AC Link Serial Interface Protocol

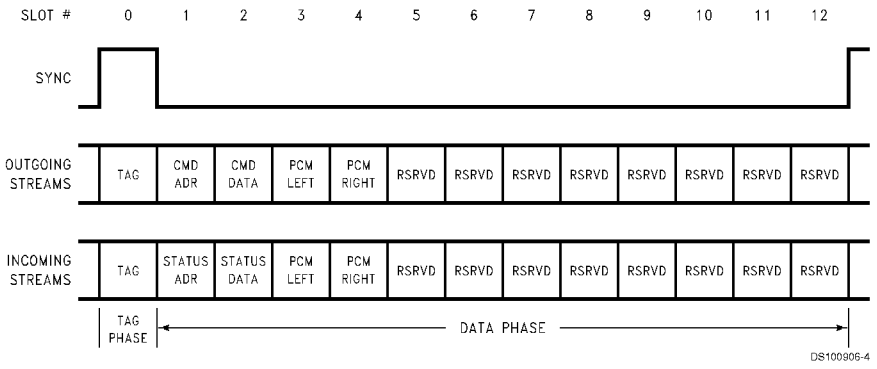



**FIGURE 3. AC 97 Bidirectional Audio Frame**

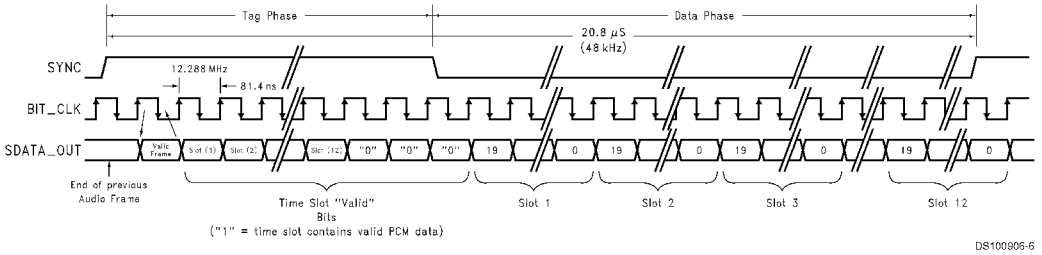



**FIGURE 4. AC Link Audio Output Frame**

### AC Link Output Frame

The audio output frame (output from AC '97 Controller) contains control and PCM data targeted for the LM4540 control register and stereo DAC. The Tag slot, slot 0, contains 16 bits that tell the AC Link interface circuitry on the LM4540 the validity of the following data slots.

A new audio output frame is signaled with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the next rising edge of BIT_CLK, the AC '97 Controller drives SD_OUT with the first bit of slot 0. The LM4540 samples SD_OUT on the falling edge of BIT_CLK. The AC '97 Controller will continue outputting the SD_OUT stream on each successive rising edge of BIT_CLK.

### SD_OUT Slot 0: Tag Phase

The first bit of slot 0 is designated the "Valid Frame" bit. If this bit is 1, it indicates that the current data frame contains at least one slot of valid data and the LM4540 will further sampled the next four bits to determine which frames do in fact have valid data. Valid slots are signified by a 1 in their respective slot bit position.

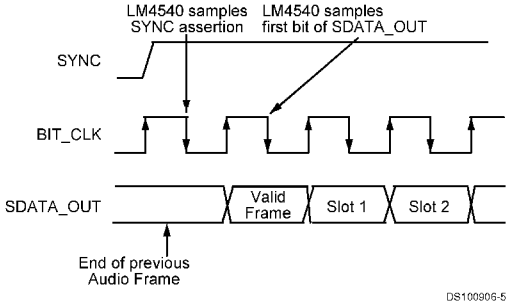



**FIGURE 5. Start of Audio Output Frame**

| Bit | Description | Comment |
|---|---|---|
| 15 | Valid Frame | 1 = Valid Frame |
| 14 | Control register address | 1 = Valid slot |
| 13 | Control register data | 1 = Valid slot |
| 12 | Left Playback PCM Data | 1 = Valid slot |

## Application Information (Continued)

| Bit | Description | Comment |
|---|---|---|
| 11 | Right Playback PCM Data | 1 = Valid slot |

**SD_OUT Slot 1: Control Address**

Slot 1 is used both to write to the LM4540 registers as well as read back a register's current value. The MSB of Slot 1 (bit 19) signifies whether the current control operation is a read or a write. Bits 18 through 12 are used to specify the register address of the read or write operation. The least significant twelve bits are reserved and should be stuffed with zeros by the AC'97 controller.

| Bits | Description | Comment |
|---|---|---|
| 19 | Read/Write | 0 = Write, 1 = Write |
| 18:12 | Control Register | Identifies the Control Register |
| 11:0 | Reserved | Set to "0" |

**SD_OUT Slot 2: Control Data**

Slot 2 is used to transmit 16 bit control data to the LM4540 in the event that the current operation is a write operation. The least significant four bits should be stuffed with zeros by the AC '97 controller. If the current operation is a register read, the entire slot, bits 19 through 0 should be stuffed with zeros.

| Bits | Description | Comment |
|---|---|---|
| 19:4 | Control Register Write Data | Set bits to "0" if read operation |
| 3:0 | Reserved | Set to "0" |

**SD_OUT Slot 3: PCM Playback Left Channel**

Slot 3 is a 20 bit field used to transmit data intended for the left DAC on the LM4540. Any unused bits should be padded with zeros. The LM4540 DAC's have 18 bit resolution and thus will use the first 18 bits of the 20 bit PCM stream.

| Bits | Description | Comment |
|---|---|---|
| 19:0 | PCM Audio Data for Left DAC | Set unused bits to "0" |

**SD_OUT Slot 4: PCM Playback Right Channel**

Slot 4 is a 20 bit field used to transmit data intended for the right DAC on the LM4540. Any unused bits should be padded with zeros. The LM4540 DAC's have 18 bit resolution and thus will use the first 18 bits of the 20 bit PCM stream.

| Bits | Description | Comment |
|---|---|---|
| 19:0 | PCM Audio Data for Right DAC | Set unused bits to "0" |

**SD_OUT Slots 5-12: Reserved**

Set these SD_OUT slots to "0" as they are not currently used and are reserved for future use.

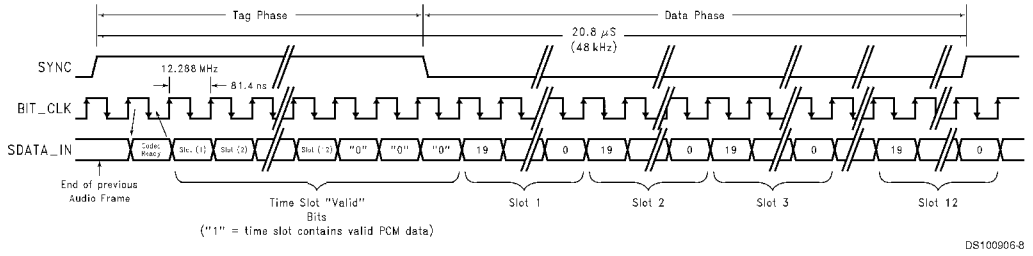



**FIGURE 6. AC Link Audio Input Frame**

**AC Link Input Frame**

The audio input frame (input to the AC '97 Digital Controller) contains status and PCM data from the LM4540 control registers and stereo ADC. The Tag slot, slot 0, contains 16 bits that tell the AC '97 Digital Controller whether the LM4540 is ready and the validity of data from certain device subsections.

A new audio input frame is signaled with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the next rising edge of BIT_CLK, the LM4540 drives SD_IN with the first bit of slot 0. The Digital Controller samples SD_IN on the falling edge of BIT_CLK. The LM4540 will continue outputting the SD_IN stream on each successive rising edge of BIT_CLK. The LM4540 outputs data MSB first, in a MSB justified format. All reserved bits and slots are stuffed with "0" 's by the LM4540.

**SD_IN Slot 0: Codec Status Bits**

The first bit of SD_IN Slot 0 (bit 15), if asserted (="1"), indicates that the Codec is ready. The digital controller must probe further to see which other subsections are ready.

## Application Information (Continued)

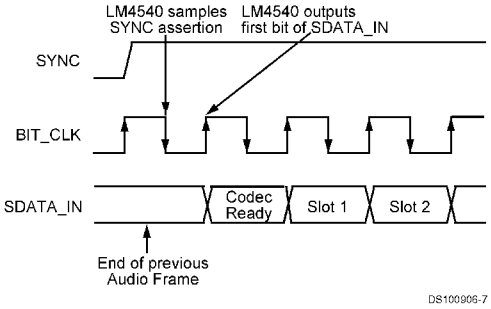



**FIGURE 7. Start of Audio Input Frame**

| Bit | Description | Comment |
|---|---|---|
| 15 | Codec Ready Bit | 0=Not Ready, 1=Ready |
| 14 | Slot 1 data valid | Status Address is valid |
| 13 | Slot 2 data valid | Status Data is valid |
| 12 | Slot 3 data valid | Left Audio PCM Data is valid |
| 11 | Slot 4 data valid | Right Audio PCM Data is valid |

### SD_IN Slot 1: Status Address

The slot echoes the control register which a read was requested on. The address echoed was initiated by a read request in the previous SD_OUT frame, slot 1.

| Bits | Description | Comment |
|---|---|---|
| 19 | Reserved | Stuffed with "0" |
| 18:12 | Control Register Index | Echo of Control Register for which data is being returned. |
| 11:0 | Reserved | Stuffed with "0" 's |

### SD_IN Slot 2: Status Data

The slot returns the control register data. The data returned was initiated by a read request in the previous SD_OUT frame, slot 1.

| Bits | Description | Comment |
|---|---|---|
| 19:4 | Control Register Read Data | |
| 3:0 | Reserved | Stuffed with "0" 's |

### SD_IN Slot 3: PCM Record Left Channel

This slot contains the left ADC sample data. The signal digitized is selected via register 1Ah and subsequently routed through the Input Mux for recording by the left ADC.

| Bits | Description | Comment |
|---|---|---|
| 19:2 | PCM Record Left Channel data | 18 bit audio sample from left ADC |
| 1:0 | Reserved | Stuffed with "0"s |

### SD_IN Slot 4: PCM Record Right Channel

This slot contains the right ADC sample data. The signal digitized is selected via register 1Ah and subsequently routed through the Input Mux for recording by the right ADC.

| Bits | Description | Comment |
|---|---|---|
| 19:2 | PCM Record Right Channel data | 18 bit audio sample from right ADC |
| 1:0 | Reserved | Stuffed with "0"s |

### SD_IN Slots 5-12: Reserved

These SD_IN slots are set to "0" as they are reserved for future use.

### AC Link Low Power Mode

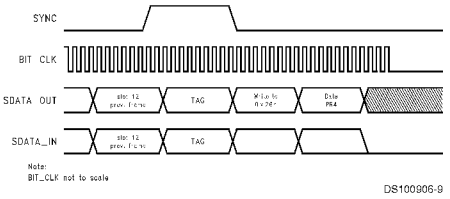



**FIGURE 8. AC Link Powerdown Timing**

### Reset Register (00h)

Writing any value to this register causes a register reset which changes all of the registers back to their default values. If this register is read, the codec will return a value of 0D50h indicating that National 3D Sound is implemented and 18 bit data is supported by both the ADCs and DACs.

### Master Volume Registers (02h, 06h)

These registers allows the output levels from LINE_OUT port and MONO_OUT port to be attenuated or muted. Each step is nominally 1.5dB and each output can be individually muted by setting the most significant bit to 1.

| Mute | Mx5:Mx0 | Function |
|---|---|---|
| 0 | 00 0000 | 0dB attenuation |
| 0 | 01 1111 | 46.5dB attenuation |
| 0 | 1X XXXX | 46.5dB attenuation |
| 1 | XX XXXX | mute |
| Default: 8000h | | |

### PC Beep Register (0Ah)

This register controls the level of the PC_BEEP input. The PC_BEEP can be both attenuated and muted via register 0Ah. Step size is nominally 3dB. The signal present after the attenuation and mute block is summed into both the left and right channels.

| Mute | PV3:0 | Function |
|---|---|---|
| 0 | 0000 | 0dB attenuation |
| 0 | 1111 | 45dB attenuation |
| 1 | XXXX | mute |
| Default: 8000h | | |

## Application Information (Continued)

**Mixer Input Volume Registers (Index 0Ch - 12h, 18h)**

These registers control the input volume controls including mute. Each volume control is 5 bit which provides from a range of +12dB gain to 34.5dB attenuation. For stereo ports, the left and right levels can be independently set. Muting a given port is accomplished by setting the MSB to 1. Setting the MSB to 1 for stereo ports mutes both the left and right channel. Register 0Eh has an additional 20dB boost for a microphone level input. This is enabled by setting bit 6 of register 0Eh to 1.

| Mute | Gx4:Gx0 | Function |
|---|---|---|
| 0 | 00000 | +12dB gain |
| 0 | 01000 | 0dB gain |
| 0 | 01111 | 34.5dB attenuation |
| 1 | XXXXX | mute |
| Default: 8008h (mono regs.), 8808h (stereo regs.) | | |

**Record Select Register (1Ah)**

This register independently controls the source for the right and left channel which will be recorded by the stereo ADC. The default value is 0000h which corresponds to Mic in.

| SL2:SL0 | Left Record Source |
|---|---|
| 0 | Mic |
| 1 | CD In (L) |
| 2 | not used |
| 3 | not used |
| 4 | Line In (L) |
| 5 | Stereo Mix (L) |
| 6 | Mono Mix (L) |
| 7 | Phone |

| SR2:SR0 | Right Record Source |
|---|---|
| 0 | Mic |
| 1 | CD In (R) |
| 2 | not used |
| 3 | not used |
| 4 | Line In (R) |
| 5 | Stereo Mix (R) |
| 6 | Mono Mix (R) |
| 7 | Phone |

**Record (Input) Gain Register (1Ch)**

This registers controls the Record (Input) Gain level for the stereo input selected via the Record Select Control Register (1Ah). The gain can be programmed from 0dB to +22.5dB in 1.5dB steps. The level for the left and right channel can be individually controlled. The input can also be muted by setting the MSB to 1.

| Mute | Gx3:Gx0 | Function |
|---|---|---|
| 0 | 1111 | 22.5dB gain |
| 0 | 0000 | 0dB gain |
| 1 | XXXX | mute |
| Default: 8000h | | |

**General Purpose Register (20h)**

This register controls many miscellaneous functions implemented on the LM4540. The miscellaneous functions include POP which allows the PCM to bypass the National 3D Sound circuitry, 3D which enables or disables the National 3D Sound circuitry, MIX which selects the MONO_OUT source, MS which selects the microphone mux source, and LPBK which connects the output of the stereo ADC to the input of the stereo DAC. LPBK provides a digital loopthru path when enabled.

| BIT | Function |
|---|---|
| POP | PCM out path and mute, 0 = pre 3D, 1 = post 3D |
| 3D | National 3D Sound on / off 1 = on |
| MIX | Mono output select 0 = Mix, 1 = Mic |
| MS | Mic select 0 = Mic1 1 = Mic2 |
| LPBK | ADC/DAC loopback |

**Powerdown Control / Status Register (26h)**

This read/write register is used to monitor subsystem readiness and program LM4540 powerdown states. The lower half of this register is read only with a "1" indicated the subsection is ready. Writing to the lower 8 bits will have no effect.

When the AC Link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1 it indicates that the AC Link and AC '97 registers are in a fully operational state. The AC '97 Controller must further probe the Powerdown Control / Status Register to determine exactly which subsections are ready.

| BIT | Function |
|---|---|
| REF | Vref's up to nominal level |
| ANL | Analog mixers ready |
| DAC | DAC section ready to accept data |
| ADC | ADC section ready to transmit data |

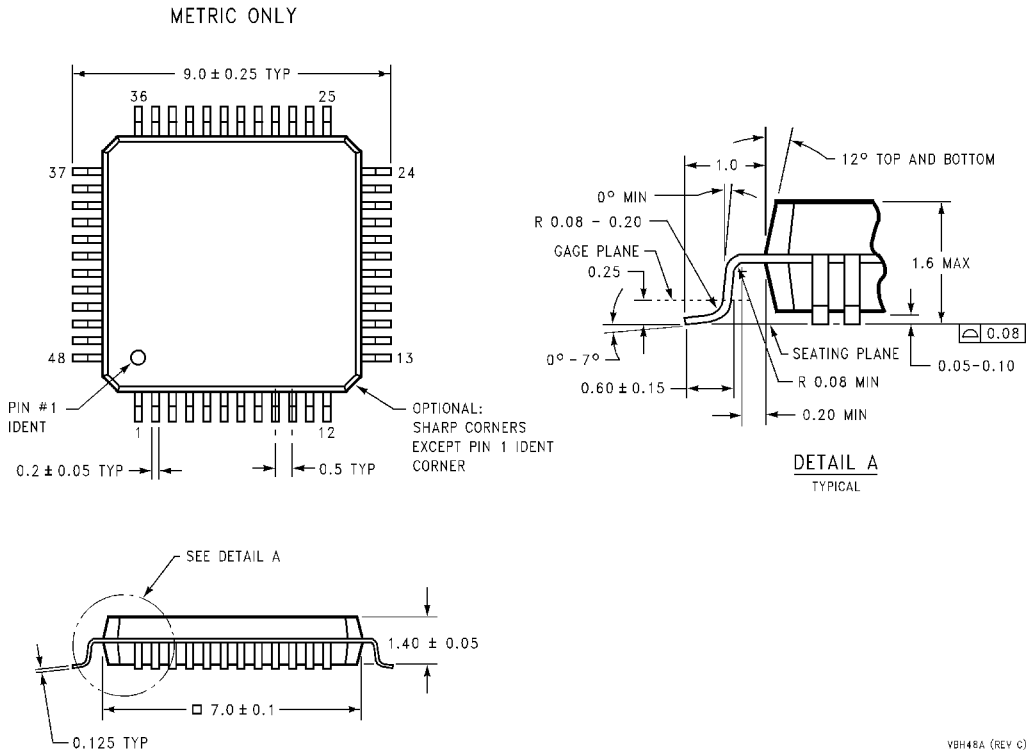
The supported powerdown modes are as follows.

| BIT | Function |
|---|---|
| PR0 | PCM in ADC's and Input Mux powerdown |
| PR1 | PCM out DAC's powerdown |
| PR2 | Analog Mixer powerdown (VREF still on) |
| PR3 | Analog Mixer powerdown (VREF off) |
| PR4 | Digital Interface (AC Link) powerdown (external clk off) |
| PR5 | Internal Clk disable |
| PR6 | not used |

**Reserved Registers (28h - 7Ah)**

Do not write to these registers as they are reserved.

## Physical Dimensions inches (millimeters) unless otherwise noted

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**Order Number LM4540VH**
**NS Package Number VBH48A**

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