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National Semiconductor

September 15, 2011

LM96570

Ultrasound Configurable Transmit Beamformer

General Description

The LM96570 is an eight-channel monolithic beamformer for pulse generators in multi-channel medical ultrasound applications. It is well-suited for use with National's LM965XX series chipset which offers a complete medical ultrasound solution targeted towards low-power, portable systems.

The LM96570 offers eight P and N output channels with individual delays of up to 102.4 µs operating at pulse rates of up to 80 MHz. A pulse sequence is launched on all channels simultaneously through a single firing signal. Advanced features include delay resolution down to 0.78 ns and programmable patterns of up to 64 pulses. Pulse patterns and delay settings are pre-programmed through a serial interface, thereby simplifying the timing requirements on the driving circuitry.

The LM96570 is packaged in a 32-pin LLP.

Applications

- Ultrasound Imaging

Features

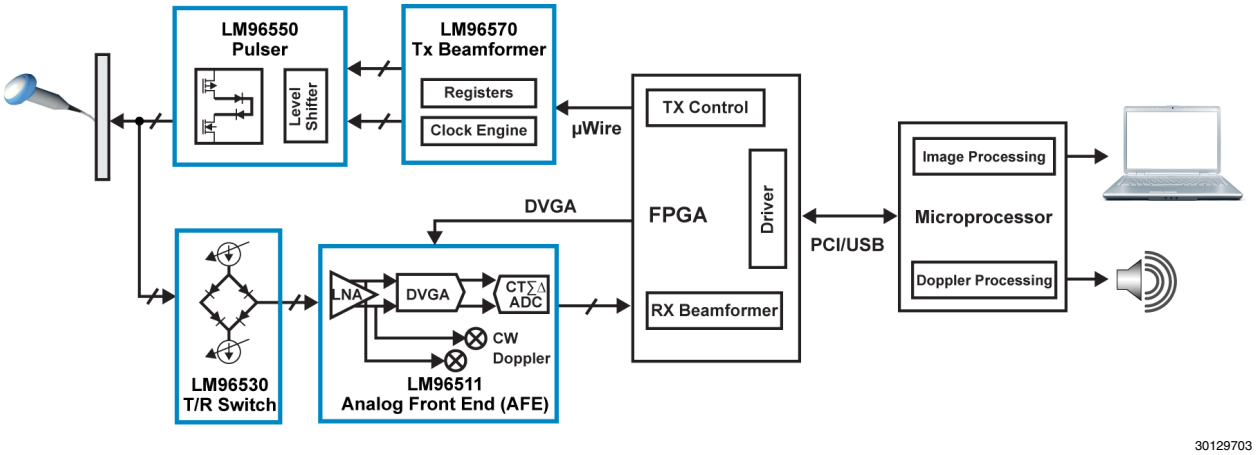
- Full control over selecting beam directions and pulse patterns by programming individual channel parameters
- Outputs interface seamlessly with positive and negative inputs on octal high-voltage pulser ICs
- Beamformer timing provides:
  - — Delay resolution of 0.78 ns
  - — Delay range of up to 102.4 µs
- Pulse patterns are locally generated with:
  - — Sequences of up to 64 pulses
  - — Adjustable Pulse widths
- 2.5V to 3.3V CMOS logic interface

Key Specifications

I/O voltage	2.5 to 3.3	V
Core supply voltage	1.8	V
Output pulse rate	80	MHz
Reference frequency	40 (±5%)	MHz
1σ Output Jitter (@ 5MHz)	25	ps
Output Phase Noise (@ 5MHz, 1kHz offset)	–116	dBc/Hz
Delay resolution	0.78	ns
Delay range	102.4	µs
Max. pattern length	64	pulses
Serial interface speed	80	Mbps
Total Power	0.063	Watts
Operating Temp.	0 to +70	°C

Typical Application

8-Channel Transmit/Receive Chipset



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Connection Diagram

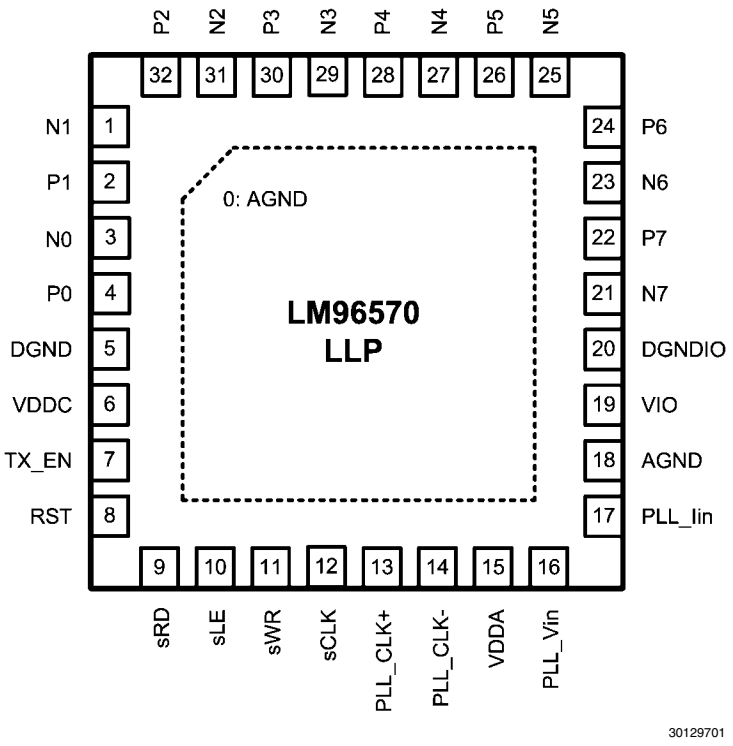


FIGURE 1. Pin Diagram of LM96570

Ordering Information

Part Number	Package	NSC Drawing	Quantity
LM96570SQ	32–Lead LLP	SQA32A	1000
LM96570SQE			250
LM96570SQX			4500

Pin Descriptions

Pin No.	Name	Type	Function and Connection
1 – 4, 21 – 32	P0-7, N0-7	Output	Control signals for pulser. P outputs control positive pulses and N outputs control negative pulses. See logic *Table 1*.
13	PLL_CLK+	Input	PLL Reference Clock PLUS Input, LVDS compatible or Single-Ended LV CMOS input, programmable through 4-Wire Serial Interface (Register 1Bh[0])
14	PLL_CLK-	Input	PLL Reference Clock MINUS input, LVDS compatible. For Single-Ended PLL Reference Clock operation, tie this pin to AGND or VDDA.
7	TX_EN	Input	1 = Beamformer starts firing 0 = Beamformer ceases firing
16	PLL_Vin	Input	Voltage range 0.8-1.2V for tuning internal PLL noise performance. Under normal conditions, 0.94V is recommended.
17	PLL_Iin	Input	100 µA current input
8	RST	Input	Asynchronous Chip Reset 1 = Reset 0 = No Reset
12	sCLK	Input	4-Wire Serial Interface Clock
10	sLE	Input	4-Wire Serial Interface Latch Enable
11	sWR	Input	4-Wire Serial Interface Data Input for writing data registers
9	sRD	Output	4-Wire Serial Interface Data Output for reading data registers
15	VDDA	Power	Analog supply voltage (1.8V)
6	VDDC	Power	Digital core supply voltage (1.8V)
19	VIO	Power	Digital I/O supply voltage (2.5 to 3.3V)
0, 18	AGND	Ground	PLL Analog ground
5	DGND	Ground	Digital core ground
20	DGNDIO	Ground	Digital I/O ground

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (*Note 4*)

Human Body Model	2kV
Machine Model	200V
Charge Device Model	750V
Maximum Junction Temperature (T_{JMAX})	+150°C
Storage Temperature Range	−40°C to +125°C
Supply Voltage (VDDA)	−0.3V to +2.0V
Supply Voltage (VDDC)	−0.3V and +2.0V
Supply Voltage (VIO)	−0.3V and +3.6V
Voltage at Analog Inputs	−0.3V and VDDA+0.3V
Voltage at Logic Inputs	−0.3V and VIO+0.3

Operating Ratings (*Note 1*)

Operating Temperature Range(T_A)	0°C to + 70°C
VDDA, Analog Supply	+1.71V to +1.89V
VDDC, Digital Core Supply	+1.71V to +1.89V
VIO, Digital IO Supply	+2.37 to +3.47
Package Thermal Resistance (θ_{JA}) (*Note 3*)	37°C/W

Analog Electrical Characteristics

Unless otherwise stated, the following conditions apply VIO = +3.3V, VDDA = VDDC = +1.8V, T_A = 25°C.

Pin	Parameter	Conditions	Min	Typ	Max	Units
	PLL Phase Noise	5MHz pulse rate, 1kHz offset		−116		dBc/Hz
VDDA	Power Supply Current	Register with No Pattern (08h - 19h)			18.5	mA
VDDC					2.4	
VIO					0.3	
VDDA	Power Supply Current	Register Default Pluse Pattern (08h - 19h), TX_EN = 15 kHz, Pulse rate = 5 MHz		16.0		mA
VDDC				6.50		
VIO				13.4		
PLL_CLK+	PLL Reference Clock Frequency		38	40	42	MHz

Beamformer Output Timing Characteristics

Unless otherwise stated, the following conditions apply VIO = +3.3V, VDDA = VDDC = +1.8V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Output Pulse Rate		0.625		80	MHz
	Output Delay Range			102.4		µs
	Output Delay Resolution			0.78		ns
	Output Pattern Length				64	Pulses
t_{OD}	Output Propagation Delay	Delay Profile (00−07h) = 0 Asynchronous TX_EN	32		47.5	ns
$t_{R/F}$	Output Rise/Fall	I_{LOAD} = 2mA		0.5	1.9	ns

Digital Electrical Characteristics

Unless otherwise stated, the following conditions apply VIO = +3.3V, VDDA = VDDC = +1.8V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLL DIFFERENTIAL REFERENCE CLOCK DC SPECIFICATIONS						
V_{ID}	PLL Reference Clock Differential Input Amplitude	AC Coupled to pins 13 & 14. 1B[0] = 0 (see (*Note 2*))	200	400		mV
V_{ICM}	PLL Reference Clock Input Common Mode Voltage	Pins 13 & 14 bias voltage, VICM ≈ 0.5 X VDDA		0.9		V
R_{IN}	Single-ended Input Resistance			11		kΩ
PLL 1.8V LVCMOS SINGLE-ENDED REFERENCE CLOCK DC SPECIFICATIONS						
V_{IH}	LVCMOS Input "HI" Voltage	Pin 13. Register 1B[0] = 1	1.5			V
V_{IL}	LVCMOS Input "LO" Voltage	Pin 13. Register 1B[0] = 1			0.3	
R_{IN}	LVCMOS Input Resistance	Pin 13 = 0V or VIO		11		kΩ
3.3V I/O DC SPECIFICATIONS						
V_{IH}	Logic Input "HI" Voltage		2.2			V
V_{IL}	Logic Input "LO" Voltage				0.5	
$I_{IN-H/L}$	Input Current		–1		1	µA
V_{OH}	Logical Output "HI" Voltage	I_{OH} = 2 mA	2.9			V
V_{OL}	Logical Output "LO" Voltage	I_{OL} = 2 mA			0.34	
$I_{O-H/L}$	Logic Output Current			±10		mA

Serial Interface Timing Characteristics

Unless otherwise stated, the following conditions apply VIO = +3.3V, VDDA = VDDC = +1.8V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LES}	sLE Setup Time		1.4			ns
t_{LEH}	sLE Hold Time		1.9			
t_{LEHI}	sLE HI Time		2.4			
t_{WS}	sWR Setup Time		1.4			
t_{WH}	sWR Hold Time		2.4			
t_{RS}	sRD Data Valid Setup Time			6.3		
t_{RH}	sRD Data Valid Hold Time			6.2		
t_{SCLKR}	sCLK Rise Time			1.7		ns
t_{SCLKF}	sCLK Fall Time			1.7		
t_{SCLKH}	sCLK High Time		2.4			ns
t_{SCLKL}	sCLK Low Time		3.4			
f_{SCLK}	sCLK Frequency				80	MHz

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device can or should be operated at these limits.

Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. Guaranteed specifications and test conditions are specified in the Electrical Characteristics section. Operation of the device beyond the Operating Ratings is not recommended as it may degrade the lifetime of the device.

Note 2: The combination of common mode and voltage swing on the clock input must ensure that the positive voltage peaks are not above VDDA and the negative voltage peaks are not below AGND.

Note 3: The maximum power dissipation is a function of T_{JMAX}, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{JMAX} - T_A)/ \theta_{JA}$. All numbers apply for package soldered directly into a 2 layer PC board with zero air flow.

Note 4: Human Body Model, applicable std. JESD22–A114–C. Machine Model, applicable std. JESD22–A115–A. Field induced Charge Device Model, applicable std. JESD22–C101–C.

Timing Diagrams

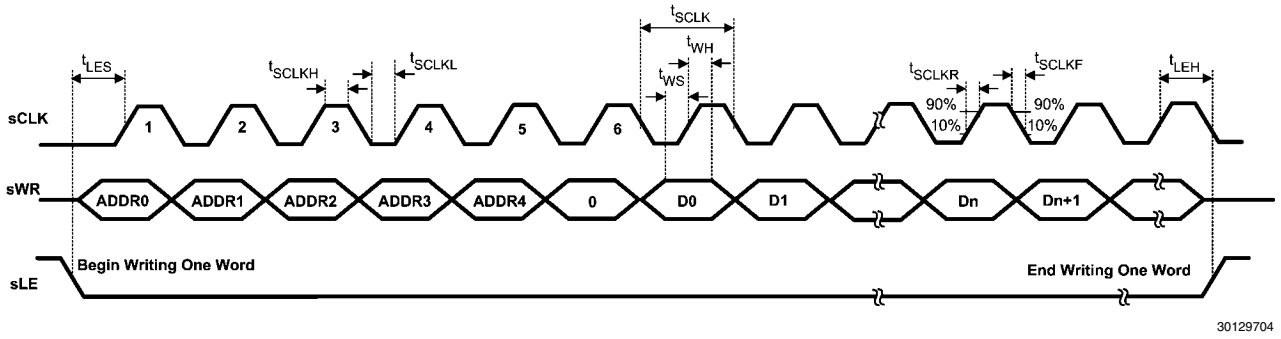


FIGURE 2. 4-Wire Serial Interface WRITE Timing

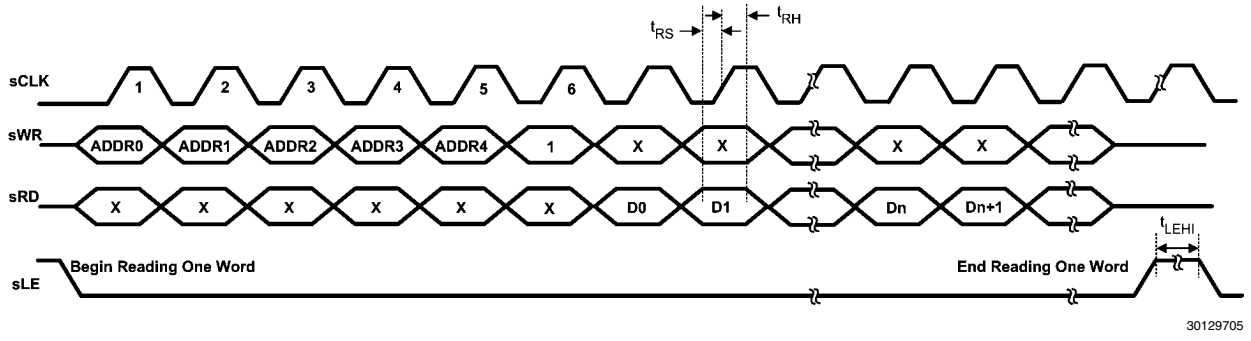
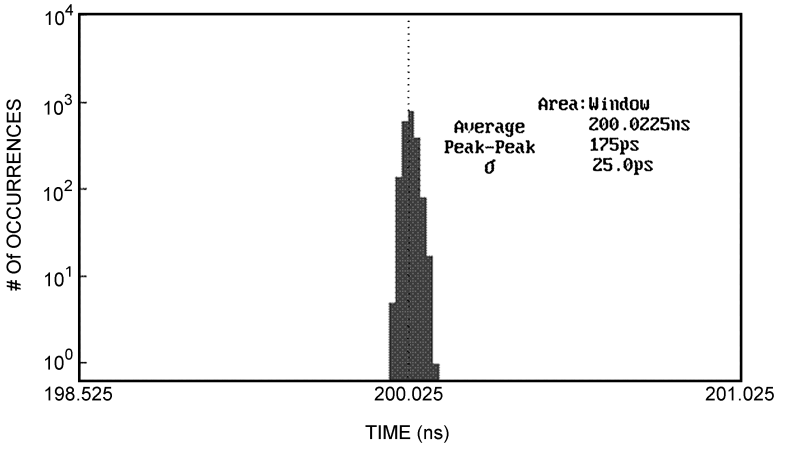


FIGURE 3. 4-Wire Serial Interface READ Timing

Typical Performance Characteristics

1δ Output Jitter



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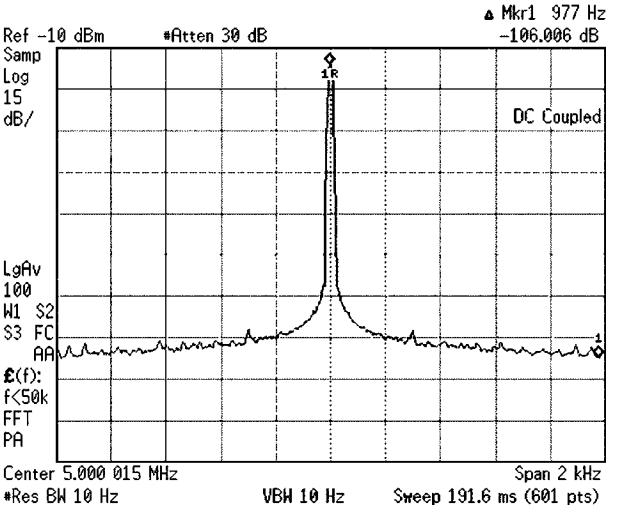
Output Phase Noise



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Overview

The LM96570 beamformer provides an 8-channel transmit side solution for medical ultrasound applications suitable for integration into multi-channel (128 / 256 channel) systems. Its flexible, integrated pulse pattern generation and delay architecture enables low-power designs suitable for ultra-portable applications. A complete system can be designed using National's companion LM9655x chipset.

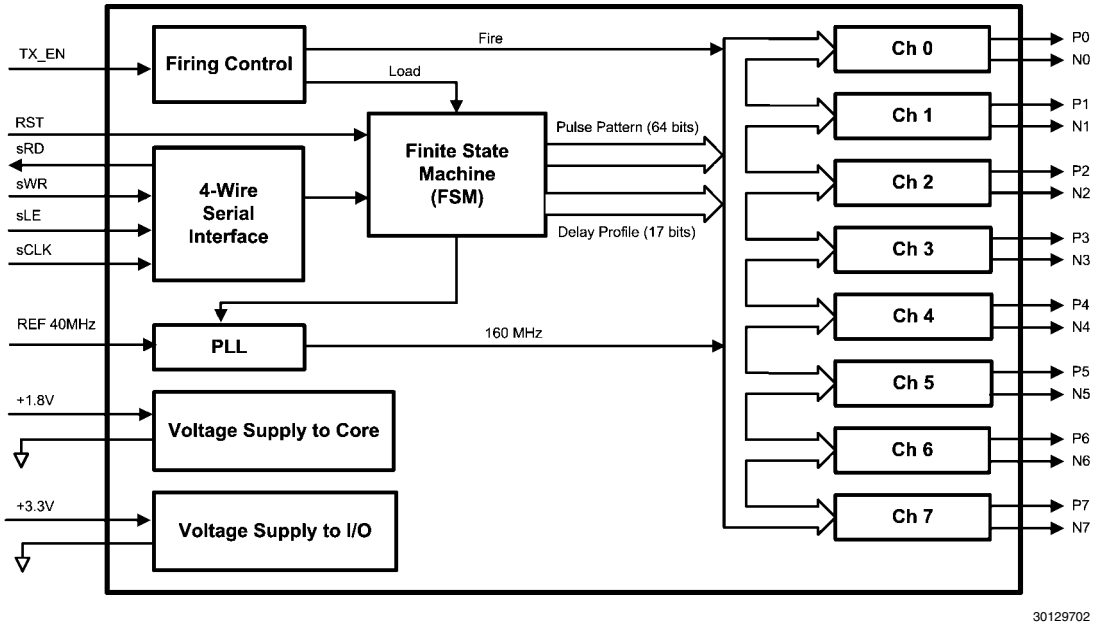


FIGURE 4. Block Diagram of Beamformer with Pattern and Delay Generator

A functional block diagram of the IC is shown in *Figure 4*. Each of the 8 output channels are designed to drive the positive and negative pulse control inputs, Pn and Nn, respectively, of a high-voltage ultrasound pulser, such as the LM96550. Upon assertion of the common firing signal, each channel launches an individually programmable pulse pattern with a maximum delay of 102.4µs in adjustable in increments of 0.78 ns. The length of a fired pulse pattern can extend up to 64 pulses. Accurate timing of the pulse generation is enabled by an on-chip PLL generating 8-phase 160 MHz internal clocks derived from an external differential or single-ended 40MHz reference.

The pulse patterns and delay settings can be programmed into and read out from the individual channel controls via a four-wire serial interface. When the Latch Enable signal (sLE) is low, the targeted on-chip registers can be written though the serial data Write pin (sWR) at the positive clock edge (sCLK). In the same way, they can also be read out through the serial data Read pin (sRD). The writing and reading operations have the same timing requirements, which are shown in *Figure 2* and *Figure 3*. The serial data stream starts with a 6-bit address, in which the first 5-bits identify the mode of updating which is interpreted by the Finite State Machine (FSM), and the sixth bit of the address indicates the 4-wire serial operation, either "WRITE" (0) or "READ" (1). The address is followed by the data word, whose length can vary from 8 bits to 64 bits. The data stream starts with the LSB and ends with the MSB. The first 5-bit address indicates which of the 27 registers is being accessed. The register map is shown in *Table 3*. In each 4-wire serial operation, only one register can be written to or read from at a time. TX_EN must be inactive during 4-wire serial interface operation.

Upon a rising edge of the transmit signal "TX_EN", the internal "Fire" signal is pulled high after an internal propagation delay relative to TX_EN elapses. Then the delay counter of each channel begins counting according to the programmable delay profile. When the counter reaches the 17-bit programmed delay value, the programmed pulse pattern is sent out continuously at the programmed frequency until it reaches the length of the pulse pattern.

The interface is compatible with CMOS logic powered at 2.5V or 3.3V. The internal core supply is derived from 1.8V referenced to 0V.

Functional Description

P/N OUTPUT PATTERN PROGRAMMING

The output pulse pattern for each of the 8 P channels is set by programming registers 08h to 0Fh, respectively. The output pulse pattern for each of the 8 N channels is set by programming registers 10h to 17h, respectively. Programming each bit of these registers yields P/N output pulses according to *Table 1*. Each bit represents one pulse, thus the full bit stream of each register is equivalent to one full length pulse pattern. However, note that the LSB of the register is transmitted as an output pulse first and the MSB is transmitted as an output pulse last. For example: a register value of "10110100" will yield an output pulse pattern versus time such as "00101101".

TABLE 1. Truth Table — Beamformer Output-to-Pulser Output

P Pattern Register Bit Value	N Pattern Register Bit Value	Beamformer P Output	Beamformer N Output	Pulser Output
0	0	0	0	0
1	0	1	0	VPP – 0.7V
0	1	0	1	VNN + 0.7V
1	1	0	0	0

If the user wishes to program the same pulse pattern for all 8 P channels or all 8 N channels, there are two additional "global channel" registers available for ease and convenience. Programming a pulse pattern via Register 18h will internally apply the same pulse pattern to all 8 P channels Similarly, programming a pulse pattern via Register 19h will internally apply the same pulse pattern to all 8 N channels.

These bit depths of these registers, i.e., pulse pattern lengths, are user-programmable via bits 0 to 2 of Register 1Ah. These 3 bits (1Ah[2:0]) determine the bit depth or pulse pattern according to *Table 2*. The outputs will not function correctly if a different number of bits, inconsistent with what is set by Register 1Ah[2:0], is programmed into any of the registers, 08h to 19h.

TABLE 2. Pulse Pattern Length Truth Table

1Ah[2:0]	Registers 08h to 19h Bit Depth	Pulse Pattern Length
000	4 bits	4 pulses
001	8 bits	8 pulses
010	16 bits	16 pulses
011	24 bits	24 pulses
100	32 bits	32 pulses
101	40 bits	40 pulses
110	48 bits	48 pulses
111	64 bits	64 pulses

DELAY ADJUSTMENT

The delay between the rising edge of the TX_EN signal and the first programmed P/N output pulse typically consists of: (1) an internal propagation delay relative to the TX_EN rising edge plus (2) a user-programmed delay value. The internal propagation delay is specified in the Beamformer Output Timing Characteristics with the programmable delay set at 0.

The user-defined delay value is set by programming the 17 Least Significant Bits in Registers 00h to 07h for each of the 8 output channels, respectively. The 17 Least Significant Bits in Delay Profile Registers 00h to 07h (00-07h[17:0]) are further divided into Coarse Delay Adjustment bits and Fine Delay Adjustment bits.

Coarse Delay Adjustment

Bits 3 to 16 (00-07h[16:3]) set the internal programmable counter, which in turn set the coarse delay value. These 14 bits control the number of internal clock cycles (ranging from 0 to 16,383) that the P/N output is delayed in addition to the internal propagation delay.

Fine Delay Adjustment

Bits 0 to 2 (00-07h[2:0]) set the clock phase for the internal programmable counter, which in turn set the fine delay value. In addition to the coarse delay, these 3 bits control the fractional amount of delay that the P/N output is delayed by relative to the internal Fire signal. The fine delay is phase adjustable in increments of 1/8 of an internal clock cycle, i.e., 45°. See *Figure 5*.

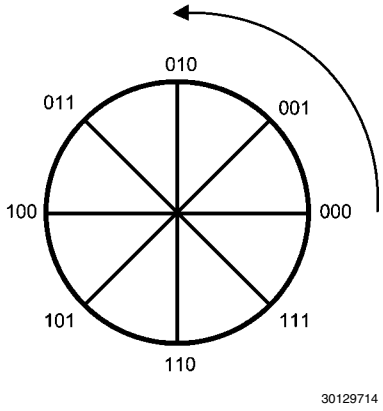


FIGURE 5. Fine Delay Adjustment (00–07h[2:0]) in 1/8 Internal Clock Phase Angle Steps

Since an internal clock cycle is 6.25 ns, the total 17-bit user-programmable delay ranges from 0 up to approximately 102.4µs.

The following example illustrates a 64-bit pulse pattern with various delay profiles. Here, the user-programmable pulse output frequency is 10 MHz. The delays are programmed such that the delay between adjacent channels is approximately 13.28 ns, which is 2 coarse delays plus one fine delay (1 coarse step or internal clock cycle = 6.25 ns & 1 fine step or 1/8 internal clock cycle = 0.78 ns).

Ch.	Register	Data	Fire Delay
Ch 0	Reg. 00h	00 000 00000000000000 000 b	no user-programmed delay
Ch 1	Reg. 01h	00 000 00000000000010 001 b	2 coarse delays + 1 fine delay
Ch 2	Reg. 02h	00 000 00000000000100 010 b	4 coarse delays + 2 fine delay
Ch 3	Reg. 03h	00 000 00000000000110 011 b	6 coarse delays + 3 fine delay
Ch 4	Reg. 04h	00 000 00000000001000 100 b	8 coarse delays + 4 fine delay
Ch 5	Reg. 05h	00 000 00000000001010 101 b	10 coarse delays + 5 fine delay
Ch 6	Reg. 06h	00 000 00000000001100 110 b	12 coarse delays + 6 fine delay
Ch 7	Reg. 07h	00 000 00000000001110 111 b	14 coarse delays + 7 fine delay

Here, the pulse pattern may be programmed to each individual channel via Registers 08h to 0Fh for the P channels and 10h to 17h for the N channels with the following 64 bits of data (shown in hexadecimal format).

Channel	Register	Data
P part Ch 0 - 7	Reg. 08h - 0Fh	5555 5555 5555 5555 h
N part Ch 0 - 7	Reg. 10h - 17h	AAAA AAAA AAAA AAAA h

Alternatively, since these 8 channels have the same pulse patterns, they can also be programmed directly to Register 18h (P part of pulse pattern) and Register 19h (N part of pulse pattern) instead of writing the same pulse pattern to each individual channel 8 times.

Channel	Register	Data
P part Ch 0 - 7	Reg. 18h	5555 5555 5555 5555 h
N part Ch 0 - 7	Reg. 19h	AAAA AAAA AAAA AAAA h

Figure 6 shows the Beamformer channel outputs and TX_EN timing. After the internal propagation delay has elapsed, each channel counts its programmed delay value. When it reaches this value, it will transmit the programmed pulse pattern. Channel 0, which has no user-programmed delay, outputs first and then is followed by Channel 1 after 2 coarse delays plus one fine delay (13.28 ns). Each bit of the 64-bit register's pulse pattern is continuously transmitted from its LSB to MSB until all 64 bits are output.

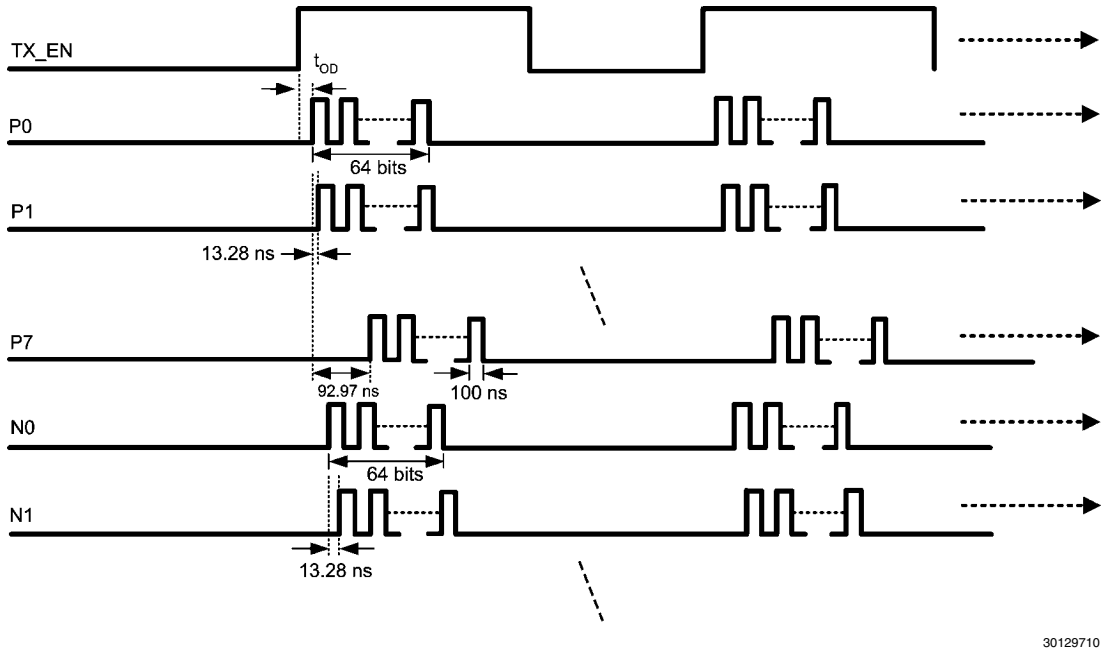


FIGURE 6. Beamformer Output Example

PULSE WIDTH ADJUST

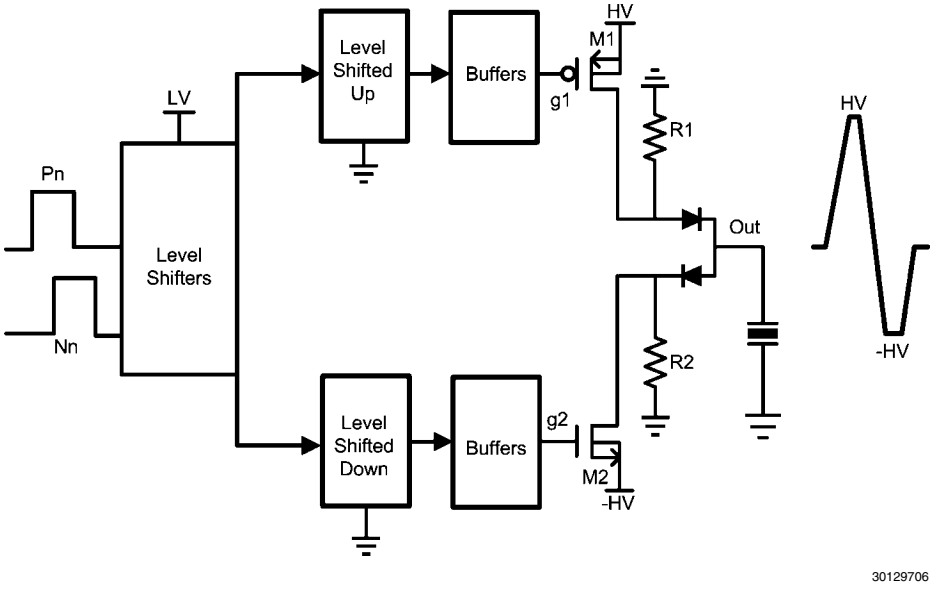


FIGURE 7. High-Voltage Pulser

Figure 7 is a diagram for a high-voltage pulser such as the LM96550. The input control signals Pn/Nn are provided by the beamformer output. These signals are level shifted up/down to the high voltage "HV"/"-HV" and buffered to drive the output stage of M1/M2 to generate high-voltage outputs. High linearity and low distortion are typically required for pulser outputs. To achieve this, the duty cycles of output pulses should be as close to 50% as possible. Due to the non-ideal nature and differences between the two signal paths, from Pn to g1, and from Nn to g2, it is very difficult achieve an ideal 50% duty cycle at the pulser outputs, even if the Pn and Nn inputs are perfectly at equal pulse width.

To address this challenge, the LM96570 can tune the pulse width of its outputs Pn/Nn to compensate the path difference, as shown in *Figure 8*. In the ideal case, the pulse width of Pn and Nn is equal, tp1'=tp2', and the corresponding pulser output duty cycle is 50%, tp1=tp2. However, in the typical case, tp1 is not equal to tp2; instead, for example, tp1>tp2. The LM96570 can then change the pulse width of Pn and Nn so that tp1'<tp2' to compensate for the difference, thus making

tp1=tp2. (See the right half of *Figure 8*.) Since Pn and Nn and low-voltage signals, it is much easier to control their timing.

After such pulse width adjustments are made, the output of the pulser will have the desired duty cycle.

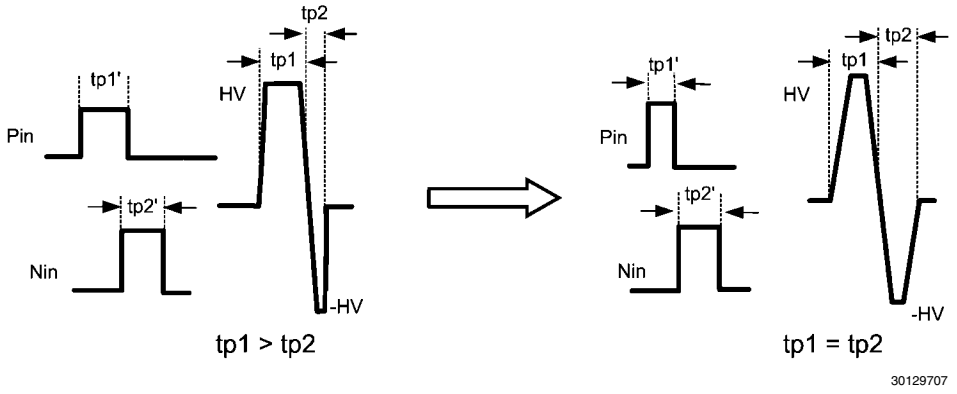


FIGURE 8. Duty Cycle Adjustment

Pulse Width Adjustment is achieved indirectly by exploiting the fact that the P and N pulses never overlap and by manipulating the phase delays of the P and N outputs relative to each other. For example, delaying P relative to N will reduce the pulse width of P and increase the pulse width of N. Similarly, delaying N relative to P will reduce the pulse width of N and increase the pulse width of P. Thus, adjusting the relative P to N phase delay essentially has the effect of adjusting the P and N pulse widths.

Bits 20 and 21 of Registers 00h to 07h enable the Pulse Width Adjustment feature and also specify which output (P or N) is to be phase delayed relative to the other according to the following table:

00-7h[21:20]	
00	Pulse Width Adjustment Disabled, i.e., each channel's P and N outputs are latched out by the same clock.
01	N Output Pulse Width Adjustment Enabled, i.e., N is delayed, while P remains undelayed. As a result, because the P and N outputs never overlap, N's pulse width decreases, while P's pulse width increases.
10	P Output Pulse Width Adjustment Enabled, i.e., P is delayed, while N remains undelayed. As a result, because the P and N outputs never overlap, P's pulse width decreases, while N's pulse width increases.
11	Pulse Width Adjustment Disabled, i.e., each channel's P and N outputs are latched out by the same clock.

Bits 17 to 19 of Registers 00h to 07h determine the amount of relative P to N phase delay, and vice-versa. These 3 bits (00-07h[19:17]) set the alternative clock phase by which the output (P or N) will lag. For example, if P Pulse Width Adjust is enabled for Channel 1 (00h[21:20] = “10”), then the 3 bits (00h[19:17]) set the alternative clock phase by which the P output will lag relative to the N output, which clock phase is still set by 00h[2:0].

The pulse width adjusted output is delayed relative to the other output according to the following phase angle / internal clock fractional step diagram. The relative delay, t_{RD}, is determined by phase lag of the alternative clock phase with reference to the original clock phase set by bits 0 to 2. If bits 17 to 19 are the same as bit 0 to 3, the relative delay is 360°, which is equivalent to one step of coarse delay, i.e. t_{RD} is one system clock period, 6.25ns.

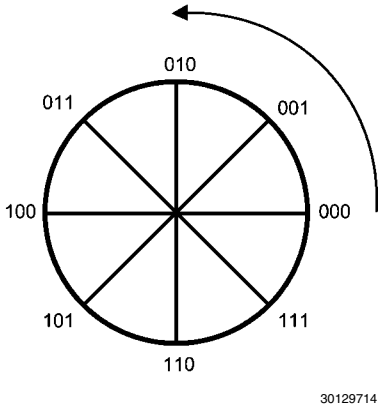


FIGURE 9. Pulse Width Adjustment (00–07h[19:17])

in 1/8 Internal Clock Phase Angle Steps

Figure 10 illustrates the Pulse Width Adjust operation in further detail. In this example, 00h[21:20] = “01”. Internally both original P and original N have an alternative phase version that lags their original phase version. Alternative phase is set by the value in 00h[19:17]. The P output is the OR’d result of the original P with the internally delayed P', while the N output is the AND’d result of the original N with the internally delayed N'. The outcome is: (1) the N output is delayed, while the P output remains undelayed; (2) the P output pulse width has increased, while the N output pulse width has decreased.

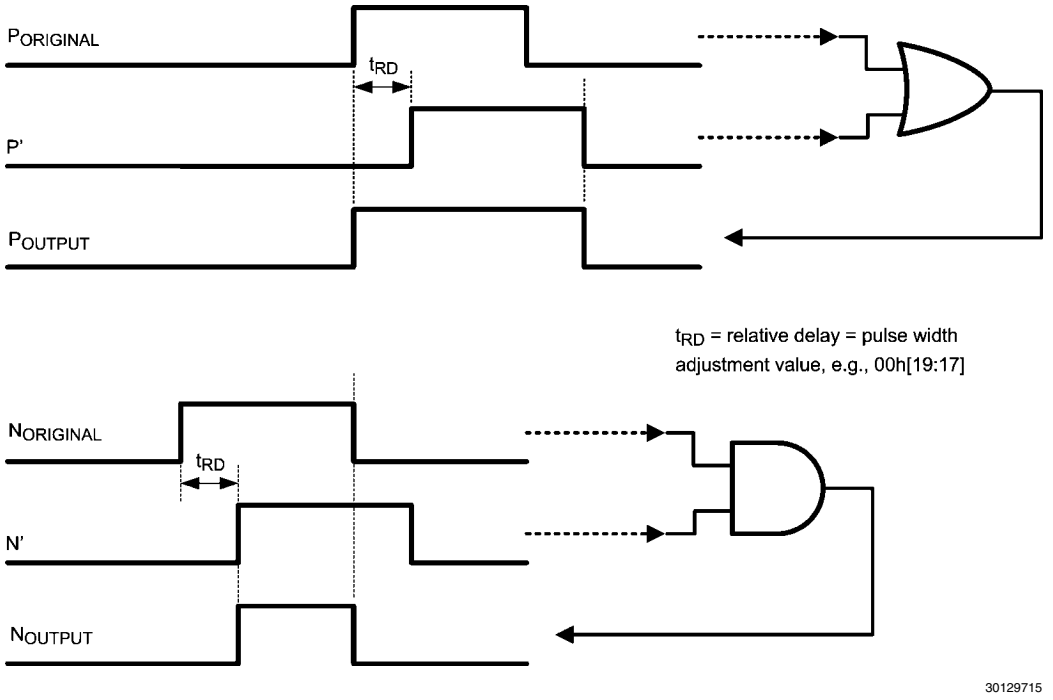


FIGURE 10. Pulse Width Adjustment (00h[21:20] = “01”)

Figure 11 illustrates a similar example, where 00h[21:20] = “10”. Here, the P output is the AND’d result of the original P with the internally delayed P', while the N output is the OR’d result of the original N with the internally delayed N'. The outcome is: (1) the P output is delayed, while the N output remains undelayed; (2) the P output pulse width has decreased, while the N output pulse width has increased.

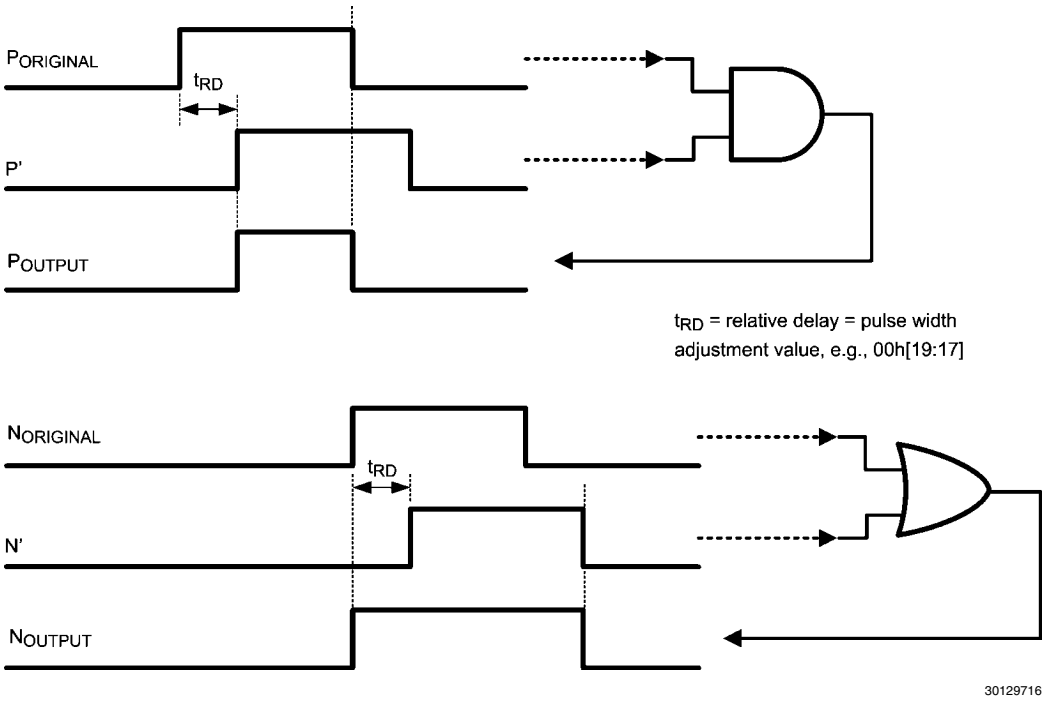


FIGURE 11. Pulse Width Adjustment (00h[21:20] = "10")

In the case where Pulse Width Adjustment is enabled and a Fire Delay Profile is programmed, the total output delay relative to the TX_EN signal for the Pulse Width Adjusted output is [the internal propagation delay] + [the programmed delay value] + [pulse width adjustment value] and the total output delay for the other output is just [the internal propagation delay value] + [the programmed delay]. The following example illustrates this in further detail. Here, the Pulse Width Adjust feature is enabled for each Channel. Channels 0 to 7 are programmed such that each P output fires 1/2/3/4/5/6/7/0 fine delays later than the N output and its pulse width is smaller than the N output by 2/4/6/8/10/12/14/0 fine delays, individually.

Ch.	Register	Data	Programmed Fire Delay	Actual Fire Delay*	P to N Delay & P's Pluse Width
Ch 0	Reg. 00h	10 001 00000000000000 000 b	ND	P: 1FD N: ND	P fires 1FD later than N. P's pulse width is smaller than N by 2FDs.
Ch 1	Reg.01h	10 011 00000000000010 001 b	2CD + 1FD	P: 2CD + 3FD N: 2CD + 1FD	P fires 2FDs later than N. P's pulse width is smaller than N by 4FDs.
Ch 2	Reg. 02h	10 101 00000000000100 010 b	4CD + 2FD	P: 4CD + 5FD N: 4CD + 2FD	P fires 3FDs later than N. P's pulse width is smaller than N by 6FDs.
Ch 3	Reg. 03h	10 111 00000000000110 011 b	6CD + 3FD	P: 6CD + 7FD N: 6CD + 3FD	P fires 4FDs later than N. P's pulse width is smaller than N by 8FDs.
Ch 4	Reg. 04h	10 001 00000000001000 100 b	8CD + 4FD	P: 9CD + 1FD N: 8CD + 4FD	P fires 5FDs later than N. P's pulse width is smaller than N by 10FDs.
Ch 5	Reg. 05h	10 011 00000000001010 101 b	10CD + 5FD	P: 11CD + 3FD N: 10CD + 5FD	P fires 6FDs later than N. P's pulse width is smaller than N by 12FDs.
Ch 6	Reg. 06h	10 101 00000000001100 110 b	12CD + 6FD	P: 13CD + 5FD N: 12CD + 6FD	P fires 7FDs later than N. P's pulse width is smaller than N by 14FDs.

Ch.	Register	Data	Programmed Fire Delay	Actual Fire Delay*	P to N Delay & P's Pluse Width
Ch 7	Reg. 07h	00 111 00000000001110 111 b	14CD + 7FD	N: 14CD + 7FD	P fires at the same time as N. P's pulse width is the same as N.
				P: 14CD + 7FD	

*** These delays do not include the internal propagation delay relative to the TX_EN rising edge. See Beamformer Output Timing Characteristics.**

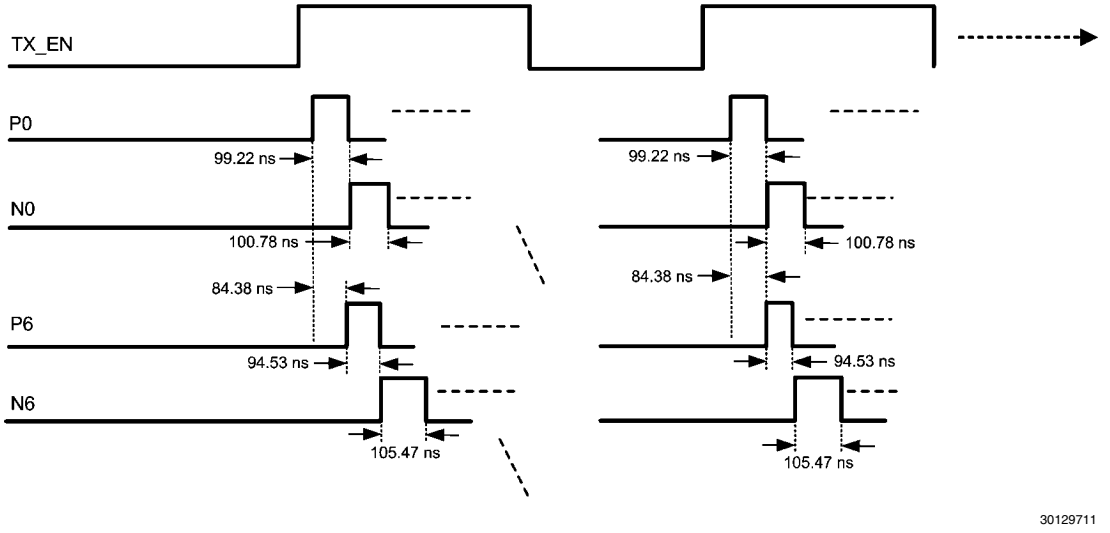


FIGURE 12. Beamformer Output with Pulse Width Adjustment

TABLE 3. Register Map

Address	Number of Bits	Default Value (binary / hex)
Individual Channel (0 to 7) Delay and Pulse Width Profile Registers		
00h	22	00 000 00000000000000 000 b
01h		00 000 00000000000010 001 b
02h		00 000 00000000000100 010 b
03h		00 000 00000000000110 011 b
04h		00 000 00000000001000 100 b
05h		00 000 00000000001010 101 b
06h		00 000 00000000001100 110 b
07h		00 000 00000000001110 111 b
Individual Channel (0 to 7) "P" Part Pulse Pattern Registers		
08h	4, 8, 16, 24, 32, 40, 48, or 64*	5555 5555 5555 5555 h
09h		
0Ah		
0Bh		
0Ch		
0Dh		
0Eh		
0Fh		
Individual Channel (0 to 7) "N" Part Pulse Pattern Registers		
10h	4, 8, 16, 24, 32, 40, 48, or 64*	AAAA AAAA AAAA AAAA h
11h		
12h		
13h		
14h		
15h		
16h		
17h		
ALL Channels "P" Part Pulse Pattern Register		
18h	4, 8, 16, 24, 32, 40, 48, or 64*	5555 5555 5555 5555 h
ALL Channels "N" Part Pulse Pattern Register		
19h	4, 8, 16, 24, 32, 40, 48, or 64*	AAAA AAAA AAAA AAAA h
Top Control Register		
1Ah	14	0001 0001111 111 b
PLL Input Clock Selection Register		
1Bh	8	0000 0000 b

*** The bit depth of registers 08h to 19h may range from 4 to 64 bits depending on the pattern length value that is programmed in Register 1Ah[2:0].**

Register Definitions

INDIVIDUAL CHANNEL (0 to 7) DELAY PROFILE REGISTERS

Address: 00h to 07h

Registers 00h to 07h control the individual delay profile and Pulse Width adjustments for channels 0 to 7, respectively.

	b[21:20]		b[19:17]			b[16:3]														b[2:0]		
Description	PWAE		PWA			CDA														FDA		
00h Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01h Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
02h Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
03h Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1
04h Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
05h Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1
06h Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0
07h Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1

Bit(s)	Description
21:20	**PWAE: Pulse Width Adjust Enable.** 00 Pulse Width Adjustment Disabled, i.e., each channel's P and N outputs are latched out by the same clock. 01 N Output Pulse Width Adjustment Enabled, i.e., the N outputs are latched out by a clock with a different phase from that of the P outputs. The clock used for the N output is phase delayed relative to the one for the P output, and thus, N is delayed relative to P. As a result, because the P and N outputs never overlap, N's pulse width is smaller than P's. 10 P Output Pulse Width Adjustment Enabled, i.e., the P outputs are latched out by a clock with a different phase from that of the N outputs. The clock used for the P output is phase delayed relative to the one for the N output, and thus, P is delayed relative to N. As a result, because the P and N outputs never overlap, P's pulse width is smaller than N's. 11 Pulse Width Adjustment Disabled, i.e., each channel's P and N outputs are latched out by the same clock.
19:17	**PWA: Pulse Width Adjust.** These 3 bits control the amount of phase delay of the clock that latches out the pulse width adjusted output relative to the unadjusted output. For example, if Pulse Width Adjust is enabled for the P outputs, then these 3 bits will determine the alternative clock phase that latches out the P output
16:3	**CDA: Coarse Delay Adjust.** Coarse delay is generated by a 14-bit programmable counter. These 14 bits control the number of internal clock cycles (0 to 16,384) that the P/N outputs are delayed relative to the internal Fire signal. This is not to be confused with the delays associated with Pulse Width Adjustment, which involves delaying the P outputs relative to the N output. Coarse Delay Adjustment involves delaying the firing of both P/N outputs relative to the internal Fire signal. The delay between when the user applies the TX_EN signal and when the P/N outputs are sent out = [internal propagation delay + # of ICLK cycles determined by the Coarse Delay Adjust value + # of fractional ICLK cycles determined by the Fine Delay Adjust value.] See the section on "Fire Delay" within the Functional Description for more details.

Bit(s)	Description
2:0	**FDA: Fine Delay Adjust.** These 3 bits set the clock phase for the 14-bit programmable counter, which in turn control the fractional amount of delay in increments of 1/8 for the P/N outputs relative to the internal Fire signal. Again, this is not to be confused with the delays associated with Pulse Width Adjustment, which involves delaying the P outputs relative to the N output. Fine Delay Adjustment involves delaying the firing of both P/N outputs relative to the internal Fire signal. In addition to the number of ICLK cycle delays determined by the Coarse Delay Adjust, the P/N outputs can be delayed further by the following number of fractional ICLK cycle delays: 000 0° or 0 ICLK cycle 001 45° or 1/8 ICLK cycle 100 90° or 2/8 ICLK cycle 011 135° or 3/8 ICLK cycle 100 180° or 4/8 ICLK cycle 101 225° or 5/8 ICLK cycle 110 270° or 6/8 ICLK cycle 111 315° or 7/8 ICLK cycle

INDIVIDUAL CHANNEL (0 to 7) "P" PART PULSE REGISTERS

Address: 08h to 0Fh

Registers 08h to 0Fh control the individual pulse patterns for channels 0 to 7, respectively.

	b[63:0], b[63:16], b[63:24], b[63:32], b[63:40], b[63:48], b[63:56], or b[63:60]
Description	PPP
08-0Fh Default	5555 5555 5555 5555 h

Bit(s)	Description
63:0, 63:16, 63:24, 63:32, 63:40, 63:48, 63:56, 63:60	**PPP: "P" Part Pulse Pattern.** These bits in registers 08h to 0Fh determine the "P" part pulse pattern for channels 0 to 7, respectively. Each bit represents one pulse, thus the full bit stream of each register is equivalent to one full length pulse pattern. Upon firing, the LSB is sent out first. The register's bit depth or pulse pattern length may be 64, 48, 40, 32, 24, 16, 8, or 4, depending on the value of Register 0Ah[2:0]. By default, the pulse pattern length is 64 bits deep, and the bit stream or pulse pattern is 5555 5555 5555 5555 h.

INDIVIDUAL CHANNEL (0 to 7) "N" PART PULSE REGISTERS

Address: 10h to 17h

Registers 10h to 17h control the individual pulse patterns for channels 0 to 7, respectively.

	b[63:0], b[63:16], b[63:24], b[63:32], b[63:40], b[63:48], b[63:56], or b[63:60]
Description	NPP
10-17h Default	AAAA AAAA AAAA AAAA h

Bit(s)	Description
63:0, 63:16, 63:24, 63:32, 63:40, 63:48, 63:56, 63:60	**NPP: "N" Part Pulse Pattern.** These bits in registers 10h to 17h determine the "N" part pulse pattern for channels 0 to 7, respectively. Each bit represents one pulse, thus the full bit stream of each register is equivalent to one full length pulse pattern. Upon firing, the LSB is sent out first. The register's bit depth or pulse pattern length may be 64, 48, 40, 32, 24, 16, 8, or 4, depending on the value of Register 0Ah[2:0]. By default, the pulse pattern length is 64 bits deep, and the bit stream or pulse pattern is AAAA AAAA AAAA AAAA h.

ALL CHANNELS (0 TO 7) "P" PART PULSE PATTERN REGISTER

Address: 18h

Register 18h controls the "P" part pulse pattern for all channels, 0 to 7.

	b[63:0], b[63:16], b[63:24], b[63:32], b[63:40], b[63:48], b[63:56], or b[63:60]
Description	PPPA
18h Default	5555 5555 5555 5555 h

Bit(s)	Description
63:0, 63:16, 63:24, 63:32, 63:40, 63:48, 63:56, 63:60	**PPPA: "P" Part Pulse Pattern for ALL Channels.** These bits determine the "P" part pulse pattern for ALL channels, 0 to 7. By writing a pulse pattern to register 18h, the same pulse pattern will be internally written to Registers 08h to 0Fh simultaneously, and thus the P pulses of all channels will have the same pulse pattern. By default, the pulse pattern length is 64 bits deep, and the bit stream or pulse pattern is 5555 5555 5555 5555 h.

ALL CHANNELS (0 TO 7) "N" PART PULSE PATTERN REGISTER

Address: 19h

Register 19h controls the "N" part pulse pattern for all channels, 0 to 7.

	b[63:0], b[63:16], b[63:24], b[63:32], b[63:40], b[63:48], b[63:56], or b[63:60]
Description	NPPA
19h Default	AAAA AAAA AAAA AAAA h

Bit(s)	Description
63:0, 63:16, 63:24, 63:32, 63:40, 63:48, 63:56, 63:60	**NPPA: "N" Part Pulse Pattern for ALL Channels.** These bits determine the "N" part pulse pattern for ALL channels, 0 to 7. By writing a pulse pattern to register 19h, the same pulse pattern will be internally written to Registers 10h to 17h simultaneously, and thus the N pulses of all channels will have the same pulse pattern. By default, the pulse pattern length is 64 bits deep, and the bit stream or pulse pattern is AAAA AAAA AAAA AAAA h.

TOP CONTROL REGISTER

Address: 1Ah

Register 1Ah is the basic initialization and global control register for the device.

	b[13]	b[12]	b[11]	b[10]	b[9:3]							b[2]	b[1]	b[0]
Description	RSV	CW	IFE	PLLE	FD							PL		
1Ah Default	0	0	0	1	0	0	0	1	1	1	1	1	1	1

Bit(s)	Description
13	**RSV: Reserved.** This is a reserved bit. When writing to Register 1Ah, keep this bit at "0."
12	**CW: Continuous Wave.** This bit enables the CW Mode. 0 CW Mode Disabled. The beamformer is in normal firing mode. After the programmed pulse pattern is sent out, each channel will automatically stop and await the next firing signal, i.e., TX_EN rising edge. 1 CW Mode Enabled. A default fixed pulse pattern will be stored in a circular shift register and continuously sent out until the TX_EN signal is pulled low. The pulse pattern cannot be customized in CW Mode; writing to Registers 08h to 19h will have no effect.

Bit(s)	Description
11	**IFE: Invert Fire Enable.** This bit enables the Invert Fire Mode, which is used for harmonic imaging. 0 Invert Fire Mode Disabled. The programmed pulse pattern will be fired directly. 1 Invert Fire Mode Enabled. Each TX transmission will consist of two firings. First, the programmed pulse pattern will be fired directly (non-inverted). Second, after RX is completed, the pulse pattern will be inverted and fired again. **During "invert firing" mode, there should be no write or read-back activity on the serial interface lines and the user must ensure that the sLE line remains high to prevent the invert-firing from inadvertently resetting.**
10	**PLLE: PLL Enable.** This bit enables the on-chip PLL 0 PLL Disabled 1 PLL Enabled
9:3	**FD: Frequency Division.** These bits determine the pulse width of each bit in the non-return zero output pulse pattern. The decimal value of these bits correspond to the 2X division factor between the 160 MHz master clock and the output pulse frequency a one-high-one-low pattern. For example, when the desired output frequency is 160 MHz / 2 = 80 MHz, then FD = 2 and Register 1Ah[9:3] = 000 0001. If the desired output frequency is 160 MHz / 32 = 5MHz, then FD = 32 and Register 1Ah[9:3] = 001 0000. If the desired output frequency is 160 MHz / 256 = 0.625 MHz, then FD = 256, which is the Maximum, and Register 1Ah[9:3] = 000 0000.
2:0	**PL: Pattern Length.** These bits determine the length of the pulse pattern for all channels. The pulse pattern length set in this register must coincide exactly with the actual pattern programmed to registers 08h through 17h, or registers 18h and 19h. For example, if the pattern length is set in this register to be 24 pulses, then exactly, a 24-bit value must be written into registers 08h through 17h or registers 18h and 19h. If a different number of bits/pulses is programmed into those registers, the outputs will not function correctly. 000 4-pulse pattern length. Registers 08h to 19h will have a 4-bit depth. 001 8-pulse pattern length. Registers 08h to 19h will have an 8-bit depth. 010 16-pulse pattern length. Registers 08h to 19h will have a 16-bit depth. 011 24-pulse pattern length. Registers 08h to 19h will have a 24-bit depth. 100 32-pulse pattern length. Registers 08h to 19h will have a 32-bit depth. 101 40-pulse pattern length. Registers 08h to 19h will have a 40-bit depth. 110 48-pulse pattern length. Registers 08h to 19h will have a 48-bit depth. 111 64-pulse pattern length. Registers 08h to 19h will have a 64-bit depth.

PLL CLOCK INPUT SELECTION REGISTER

Address: 1Bh

Register 1Bh determines whether the PLL input clock is to be a single-ended clock or a differential clock

	b[7:1]							b[0]
Description	RSV							PLLCK
0Bh Default	0	0	0	0	0	0	0	0

Bit(s)	Description
7:1	**RSV: Reserved.** This is a reserved bit. When writing to Register 1Bh, keep this bit at "0."
0	**PLLCK: PLL Clock.** This bit determines whether the PLL input clock is to be a single-ended LVCMOS input or a differential input. 0 Differential PLL Clock Input. 1 LV CMOS PLL Clock Input.

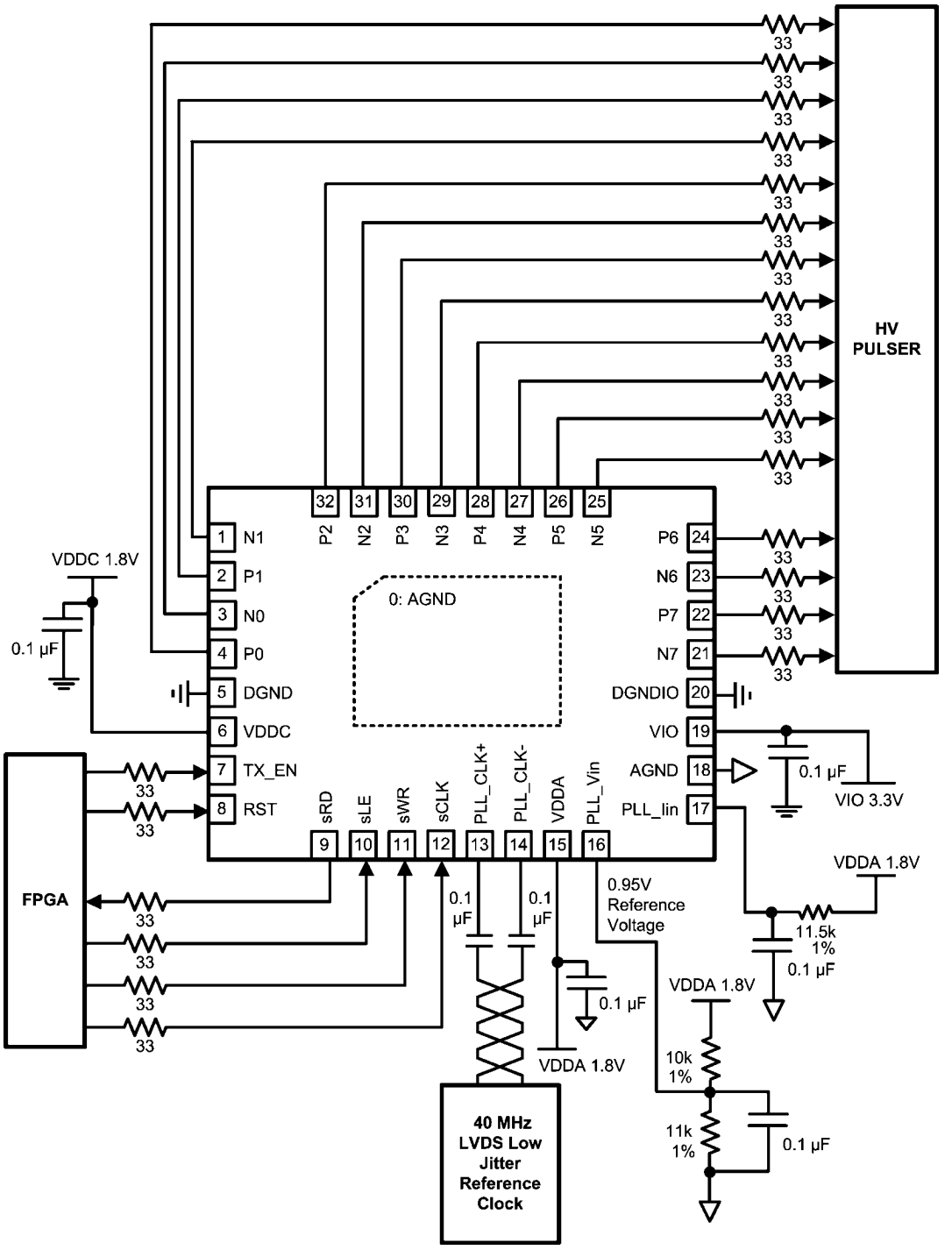


FIGURE 13. REFERENCE CIRCUIT

POWER-UP AND POWER-DOWN SEQUENCES

Power UP Sequence:

1. Turn ON VIO (pin 19) & Hold RST (pin 8) HIGH
2. Turn ON VDDA (pin 15) and VDDC (pin 6)
3. Release RST (pin 8) back to LOW
4. Set PLLE (bit 10 of register 1Ah) to LOW
5. Set PLLE (bit 10 of register 1Ah) to HIGH

Power DOWN Sequence:

1. Insure VIO (pin 19) always greater than VDDA (pin 15) & VDDC (pin 6)

FIRING SEQUENCE EXAMPLES

Example 1A (Code Excitation)

In Example 1A, a 64-bit pulse pattern is used for code excitation with the following parameters:

- Each of the eight channels have the same 64-bit pulse pattern with respect to the P part of the pattern (default 64-bit hex value = 5555 5555 5555 5555) and the N part of the pattern (default 64-bit hex value = AAAA AAAA AAAA AAAA).
- The output pulse pulse width is 100ns, 5MHz for one-on-one-off pattern.
- The delay between adjacent Channels is approximately 13.28 ns (i.e, two coarse delays with a delay step of 6.25 ns and one fine delay with a delay step of 0.78 ns). Channel 0 has no delay.
- The Pulse Width Adjust feature for all channels are disabled.

STEP 1

- Write to Register 1Ah to configure the pulse pattern length, pulse output frequency, and enable PLL. Based on the Register Definition in Table 4, here Register 1Ah (14-bit Binary) = 0001 001 0000 111 b

RESERVED	0	reserved bit is kept at “0”
CW	0	beamformer is NOT in the CW firing mode
INV_FIRE_EN	0	beamformer is NOT in the “invert firing” mode
PLL_EN	1	PLL is enabled
FREQ_DIV	001 0000	pulse width is one period of 1/16 of the master clock frequency (160MHz / 16 = 10MHz, i.e. 100ns period)
PAT_LEN	111	pulse pattern length is 64 bits.

- RESERVED (1-bit Binary) = “0” – reserved bit is kept at “0”.
- CW (1-bit Binary) = “0” – beamformer is not in the CW firing mode
- INV_FIRE_EN (1-bit Binary) = “0” – beamformer is NOT in the “invert firing” mode
- PLL_EN (1-bit Binary) = “1” – PLL is enabled.
- FREQ_DIV (7-bit Binary) = “001 0000” – 1/16 of the master clock (160MHz) for 100ns pulse width.
- PAT_LEN (3-bit Binary) = “111” – pulse pattern length is 64 bit.

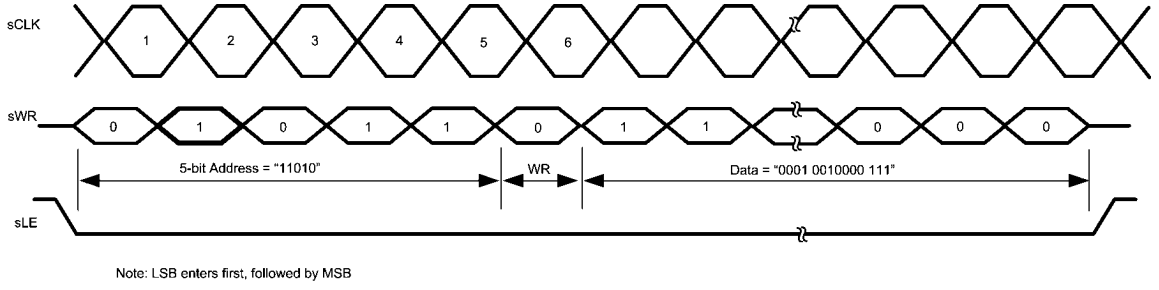


FIGURE 14. Write Register 1Ah with 14 bit = 0001 0010000 111

STEP 2.

- Write the delay profile to each Channel (Registers 00-07h) with the following 22-bit data. The write timing diagram is similar to that shown in *Figure 14*, except for the register addresses and the 22-bit data depths.

Channel	Register	Data	Fire Delay
Ch 0	Reg. 00h	00 000 00000000000000 000 b	no delay
Ch 1	Reg. 01h	00 000 00000000000010 001 b	2 coarse delays + 1 fine delay
Ch 2	Reg. 02h	00 000 00000000000100 010 b	4 coarse delays + 2 fine delay
Ch 3	Reg. 03h	00 000 00000000000110 011 b	6 coarse delays + 3 fine delay
Ch 4	Reg. 04h	00 000 00000000001000 100 b	8 coarse delays + 4 fine delay
Ch 5	Reg. 05h	00 000 00000000001010 101 b	10 coarse delays + 5 fine delay
Ch 6	Reg. 06h	00 000 00000000001100 110 b	12 coarse delays + 6 fine delay
Ch 7	Reg. 07h	00 000 00000000001110 111 b	14 coarse delays + 7 fine delay

STEP 3A.

- Write the pulse pattern to each Channel (Registers 08h to 0Fh for P and 10h to 17h for N) with the following 64 bits of data (shown in hexadecimal format). The write timing diagram is similar to *Figure 14* except for the register addresses and the 64-bit data depths.

Channel	Register	Data
P part Ch 0 - 7	Reg. 08h - 0Fh	5555 5555 5555 5555 h
N part Ch 0 - 7	Reg. 10 - 17h	AAAA AAAA AAAA AAAA h

STEP 3B (OPTIONAL instead of STEP 3A).

- Since these 8 channels have the same pulse pattern, we can also directly write to Register 18h (P part of pulse pattern) and Register 19h (N part of pulse pattern) instead of writing the same pulse pattern to each individual channel 8 times. Therefore step 3a can be replaced by step 3b.
- Write the pulse pattern to Register 18h and Registers 19h. The write timing diagram is similar to **Figure 6,** except for the register addresses and the 64-bit data depths.

Channel	Register	Data
P part Ch 0 - 7	Reg. 18h	5555 5555 5555 5555 h
N part Ch 0 - 7	Reg. 19h	AAAA AAAA AAAA AAAA h

STEP 4.

- When the write operations are complete and the TX path is ready, pull “TX_EN “ high.
- After 6 ICLK (160MHz) cycles (37.5ns) have passed, each Channel will start to count its programmed delay profile. When it reaches the preset value, it will trigger the firing sequence. Channel 0 with no delay fires first and is followed by Channel 1 after 2 coarse delays plus one fine delay (13.28ns). Each bit of the 64-bit pulse pattern is continuously fire from LSB to MSB until all 64 bits are output. “TX_EN” should always remain high during a firing operation.
- After firing is complete for all channels, “TX_EN” is pulled low, as the beamformer waits for the next firing signal, i.e., when “TX_EN” is pulled high. See *Figure 15* for firing diagram.

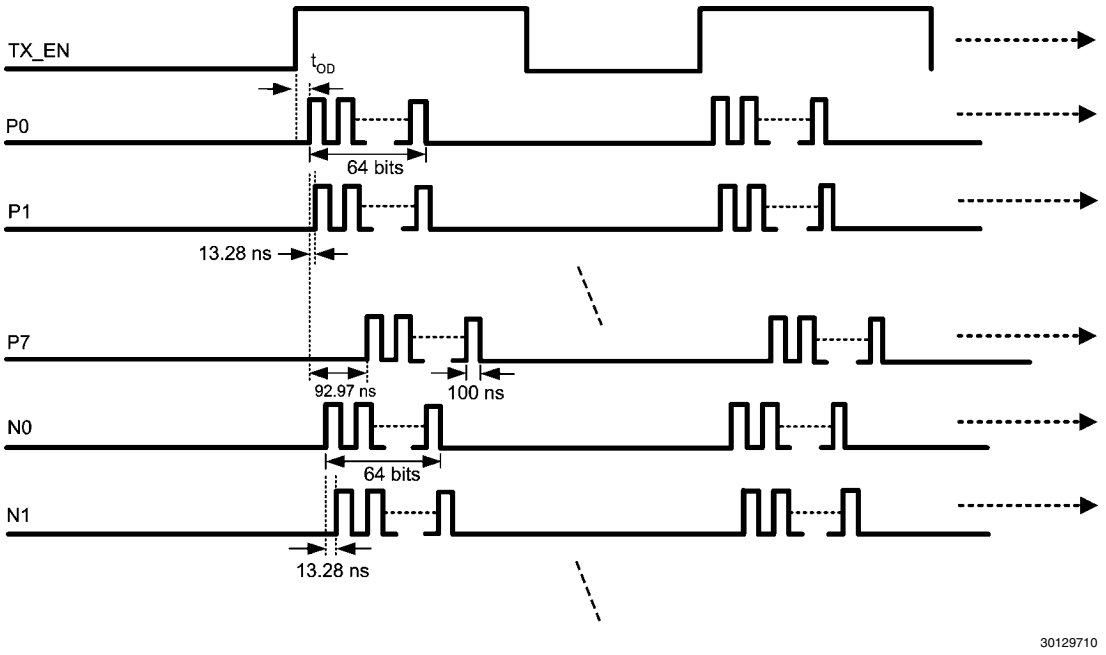


FIGURE 15. Beamformer Output with Example 1A Parameters

Example 1B (Code Excitation with Pulse Width Adjust)

Example 1B is similar to example 1A, except that the Pulse Width Adjust feature is enabled for each Channel. Channels 0 to 7 of the beamformer is programmed such that each P output fires 1/2/3/4/5/6/7/0 fine phase(s) later than the N output and its pulse width is smaller than the N output by 2/4/6/8/10/12/14/0 fine delays, individually. All of the control steps are similar to example 1A except for Step 2.

STEP 2.

Write the delay profile as well as Pulse Width Adjust information to each Channel. Here the Channel to Channel delay is the same as in example 1A; however, the Pulse Width Adjust feature for all of the channels are enabled. The P outputs and N outputs are never overlapped. See *Figure 16*.

CD = Coarse Delay, FD = Fine Delay, ND = No Delay.

Channel	Register	Data	Programmed Fire Delay	Actual Fire Delay*	P to N Delay & P's Pulse Width
Ch 0	Reg. 00h	10 001 00000000000000 000 b	ND	P: 1FD N: ND	P fires 1FD later than N. P's pulse width is smaller than N by 2FDs.
Ch 1	Reg. 01h	10 011 00000000000010 001 b	2CD + 1FD	P: 2CD + 3FD N: 2CD + 1FD	P fires 2FDs later than N. P's pulse width is smaller than N by 4FDs.
Ch 2	Reg. 02h	10 101 00000000000100 010 b	4CD + 2FD	P: 4CD + 5FD N: 4CD + 2FD	P fires 3FDs later than N. P's pulse width is smaller than N by 6FDs.
Ch 3	Reg. 03h	10 111 00000000000110 011 b	6CD + 3FD	P: 6CD + 7FD N: 6CD + 3FD	P fires 4FDs later than N. P's pulse width is smaller than N by 8FDs.
Ch 4	Reg. 04h	10 001 00000000001000 100 b	8CD + 4FD	P: 9CD + 1FD N: 8CD + 4FD	P fires 5FDs later than N. P's pulse width is smaller than N by 10FDs.
Ch 5	Reg. 05h	10 011 00000000001010 101 b	10CD + 5FD	P: 11CD + 3FD N: 10CD + 3FD	P fires 6FDs later than N. P's pulse width is smaller than N by 12FDs.

Channel	Register	Data	Programmed Fire Delay	Actual Fire Delay*	P to N Delay & P's Pulse Width
Ch 6	Reg. 06h	10 101 00000000001100 110 b	12CD + 6FD	P: 13CD + 5FD N: 12CD + 6FD	P fires 7FDs later than N. P's pulse width is smaller than N by 14FDs.
Ch 7	Reg. 07h	00 111 00000000001110 111 b	14CD + 7FD	N: 14CD + 7FD P: 14CD + 7FD	P fires at the same time as N. P's pulse width is the same as N.

* These delays do not include the internal propagation delay relative to the TX_EN rising edge. See *Beamformer Output Timing Characteristics*.

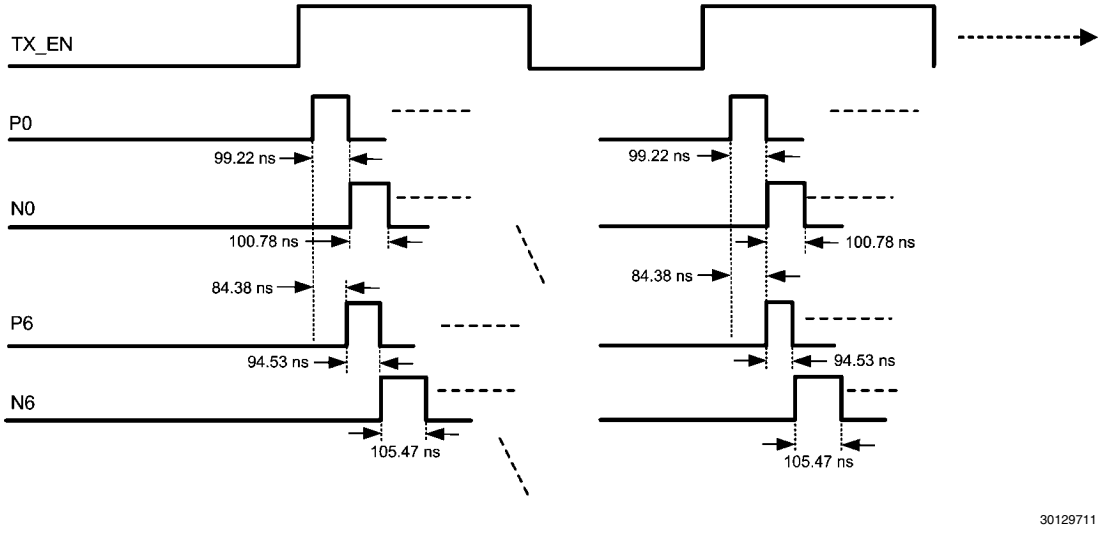


FIGURE 16. Beamformer Output with Pulse Width Adjustment

Example 2 (CW Mode)

In Example 2, the ultrasound system is in CW mode, in which a [1 0] pulse sequence for the P part and a [0 1] pulse sequence for the N part are continuously fired at a frequency of 10 MHz. **In CW mode, these P part and N part pulse sequences are fixed at pre-set default patterns, and their registers Reg. 18h and Reg. 19h CANNOT be written to.** The delay profile of each Channel is the same as in example 1. In CW mode, the pulse pattern will be fired in a circular fashion. After the last bit of the pulse pattern, the 1st bit will follow it immediately, thus configuring the pulse pattern with infinite or continuous pulse length.

STEP 1.

- Write to Register 1Ah to configure the pulse pattern length, pulse output frequency, and enable PLL. Based on the Register Definition in *TOP CONTROL REGISTER*, here Register 1Ah (14-bit) = 0101 000 1000 000 b.

RESERVED	0	reserved bit is kept at “0”
CW	1	beamformer is in the CW firing mode
INV_FIRE_EN	0	beamformer is NOT in the “invert firing” mode
PLL_EN	1	PLL is enabled
FREQ_DIV	000 1000	pulse width is one period of 1/8 of the master clock frequency (160MHz / 8 = 20MHz, i.e. 50ns period)
PAT_LEN	0	pulse pattern length is 4 bits, as 4 bits fired circularly is sufficient to generate a CW waveform.

STEP 2.

- The delay profile in example 2 is the same as in example 1A. If the beamformer is not powered down, the delay profile will be retained in the on-chip registers. Here, if the firing of example 2 immediately follows example 1A, the delay profile does not need to be written again.

STEP 3.

- When the write operations are complete and the TX path is ready, pull “TX_EN“ high. After 6 ICLK (160MHz) cycles (37.5 ns) have passed, each channel will start to count its programmed delay profile. When it reaches the preset value, it will trigger the firing sequence. TX_EN should always remain high during the firing operation. See *Figure 12* for the firing diagram.

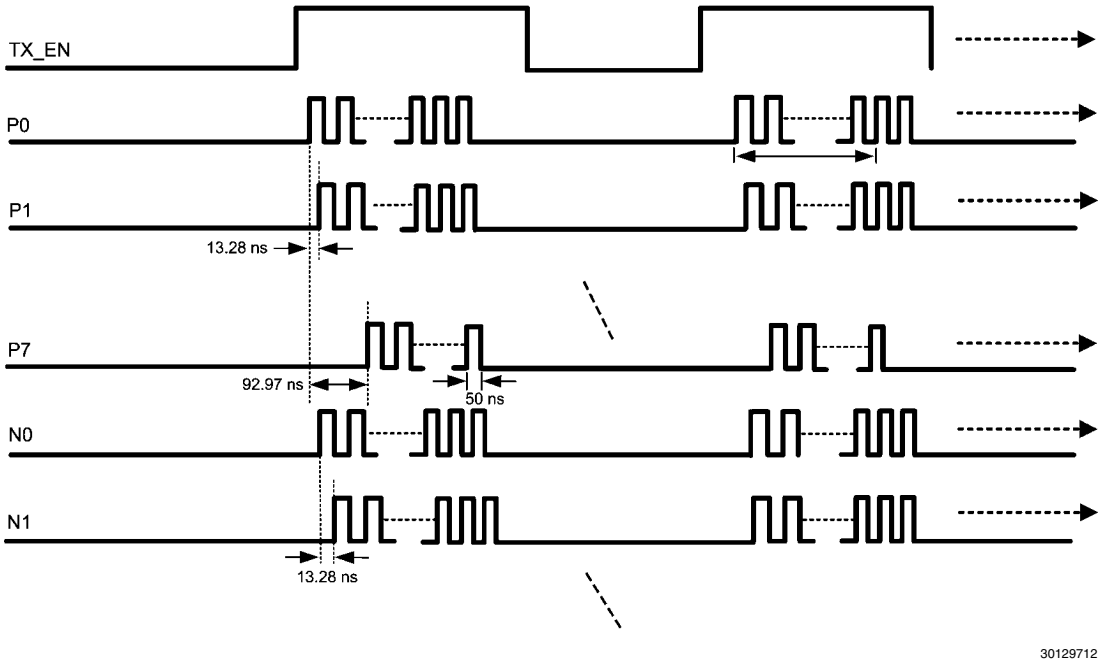


FIGURE 17. Beamformer Output in CW Mode

Example 3 (Invert Firing Mode)

Example 3 demonstrates the invert firing mode, which is used for harmonic imaging. In invert firing mode, each TX transmission consists of two firings. First, the preloaded pulse pattern will be fired directly (non-inverted). After RX is completed, in the subsequent firing, the same pulse pattern will be inverted and fired again. In this example, all Channels have zero delay, and have the same have the same unit pulse width of 50ns. The 1st firing is a non-inverted firing, in which the P pattern is “01101001” and the N pattern is “10010110”. See *Figure 18* for the firing diagram.

STEP 1.

- Write to Register 1Ah to configure the pulse pattern length, pulse output frequency, and enable PLL. Based on the Register Definition in Table 4, here Register 1Ah (14-bit) = 0011 000 1000 001 b

RESERVED	0	reserved bit is kept at “0”
CW	0	beamformer is NOT in the CW firing mode
INV_FIRE_EN	1	beamformer is in the “invert firing” mode
PLL_EN	1	PLL is enabled
FREQ_DIV	000 1000	pulse width is one period of 1/8 of the master clock frequency (160MHz / 8 = 20MHz, i.e. 50ns period)
PAT_LEN	001	pulse pattern length is 8 bits

STEP 2.

Write the delay profile to each Channel. The duty-cycle control feature is disabled.

Channel	Register	Data	Fire Delay
Ch 0 - 7	Reg. 00h - 07h	00 000 00000000000000 000 b	no delay

STEP 3.

All channels have the same pulse pattern. Write the following 8-bit pulse pattern to Register 18 and Register 19h.

Channel	Register	Data
P part Ch 0 - 7	Reg. 18h	1001 0110 b
N part Ch 0 - 7	Reg. 19h	0110 1001 b

STEP 4.

When the writing operation is complete and the TX path is ready, pull “TX_EN“ high. After 6 ICLK (160MHz) clock cycles (37.5ns) have passed, each channel will start to count its programmed delay profile. When it reaches the preset value, it will trigger the firing sequence.

As illustrated in the firing diagram in *Figure 18*, the firing begins with a non-inverted preloaded pulse pattern. After “TX_EN” is pulled low, the receiver will perform its operation. When “TX_EN” is pulled high again for the next firing, the inverted preloaded pulse pattern will be transmitted. This process will be iterated only if the beamformer is in invert firing mode.

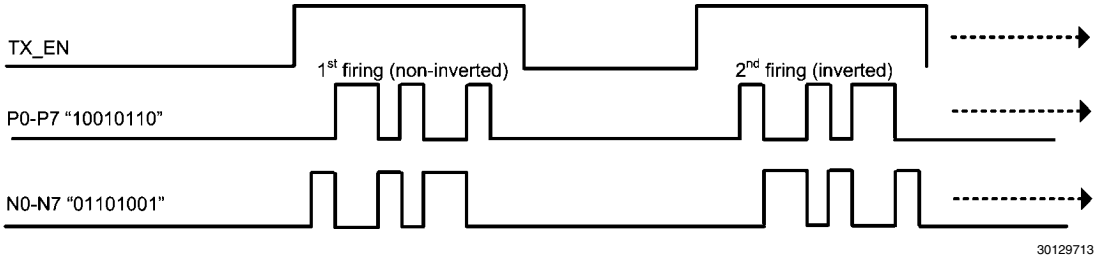
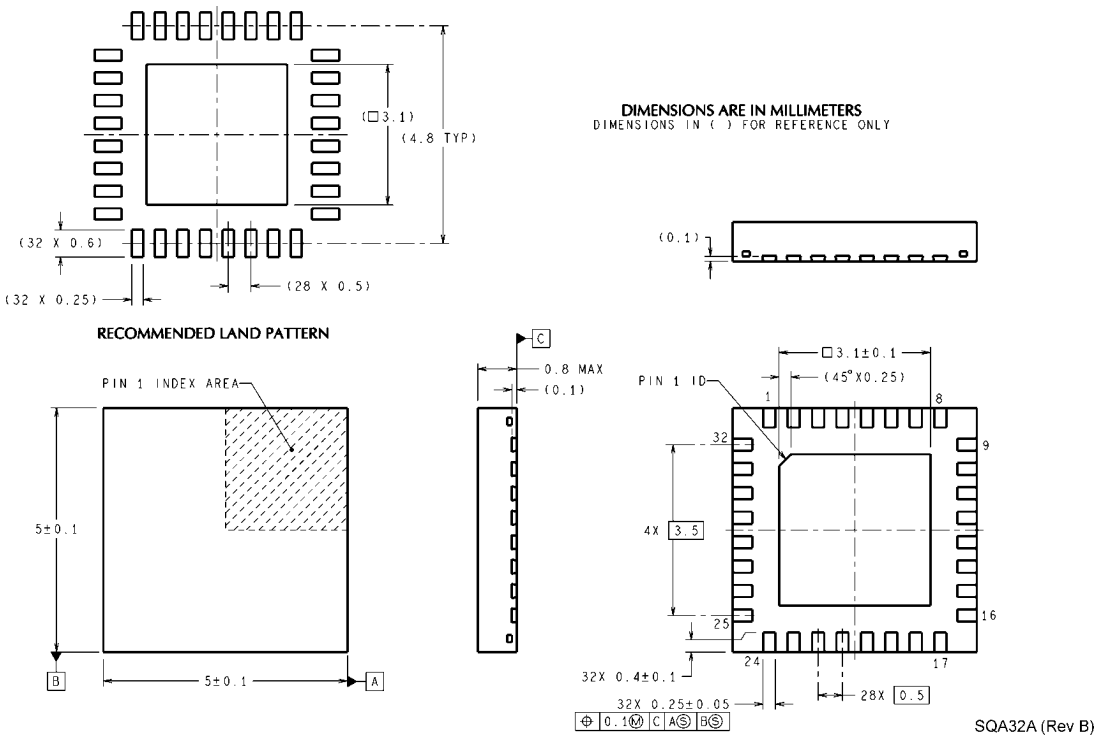


FIGURE 18. Beamformer Output in Inverting Mode

Physical Dimensions inches (millimeters) unless otherwise noted



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Notes

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LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
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