PCA9559

5-bit multiplexed/1-bit latched 6-bit I²C-bus EEPROM DIP switch

Rev. 5.0 — 25 October 2021 Product data sheet

1 General description

PCA9559 is a 20-pin CMOS device consisting of one 6-bit non-volatile EEPROM registers, 5 hardware pin inputs and a 5-bit multiplexed output with one latched EEPROM bit. It is used for DIP switch-free or jumper-less system configuration and supports Mobile and Desktop VID Configuration, where 2 preset values (1 sets of internal non-volatile registers and 1 set of external hardware pins) set processor voltage for operation in either performance or deep sleep modes. The PCA9559 is also useful in server and telecom/networking applications when used to replace DIP switches or jumpers, since the settings can be easily changed via I²C/SMBus without having to power down the equipment to open the cabinet. The non-volatile memory retains the most current setting selected before the power is turned off.

The PCA9559 typically resides between the CPU and Voltage Regulator Module (VRM) when used for CPU VID (Voltage IDentification code) configuration. It is used to bypass the CPU-defined VID values and provide a different set of VID values to the VRM, if an increase in the CPU voltage is desired. An increase in CPU voltage combined with an increase in CPU frequency leads to a performance boost of up to 7.5%. Lower CPU voltage reduces power consumption.

The PCA9559 has 2 address pins allowing up to 4 devices to be placed on the same I²C-bus or SMBus.

2 Features and benefits

- 5-bit 2-to-1 multiplexer, 1-bit latch DIP switch
- 6-bit internal non-volatile register
- Internal non-volatile register programmable and readable via I²C-bus
- Override input forces all outputs to logic 0
- 5 open drain multiplexed outputs
- 1 open drain non-multiplexed (latched) output
- 5 V and 2.5 V tolerant inputs/outputs
- Useful for ‘jumperless’ configuration of PC motherboards
- 2 address pins, allowing up to 4 devices on the I²C-bus
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA.

3 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9559PW	PCA9559	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method [1]	Minimum order quantity	Temperature
PCA9559PW	PCA9559PW,118	TSSOP20	REEL 13" Q1 NDP	2500	T_{amb} = -40 °C to +85 °C

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.

4 Block diagram

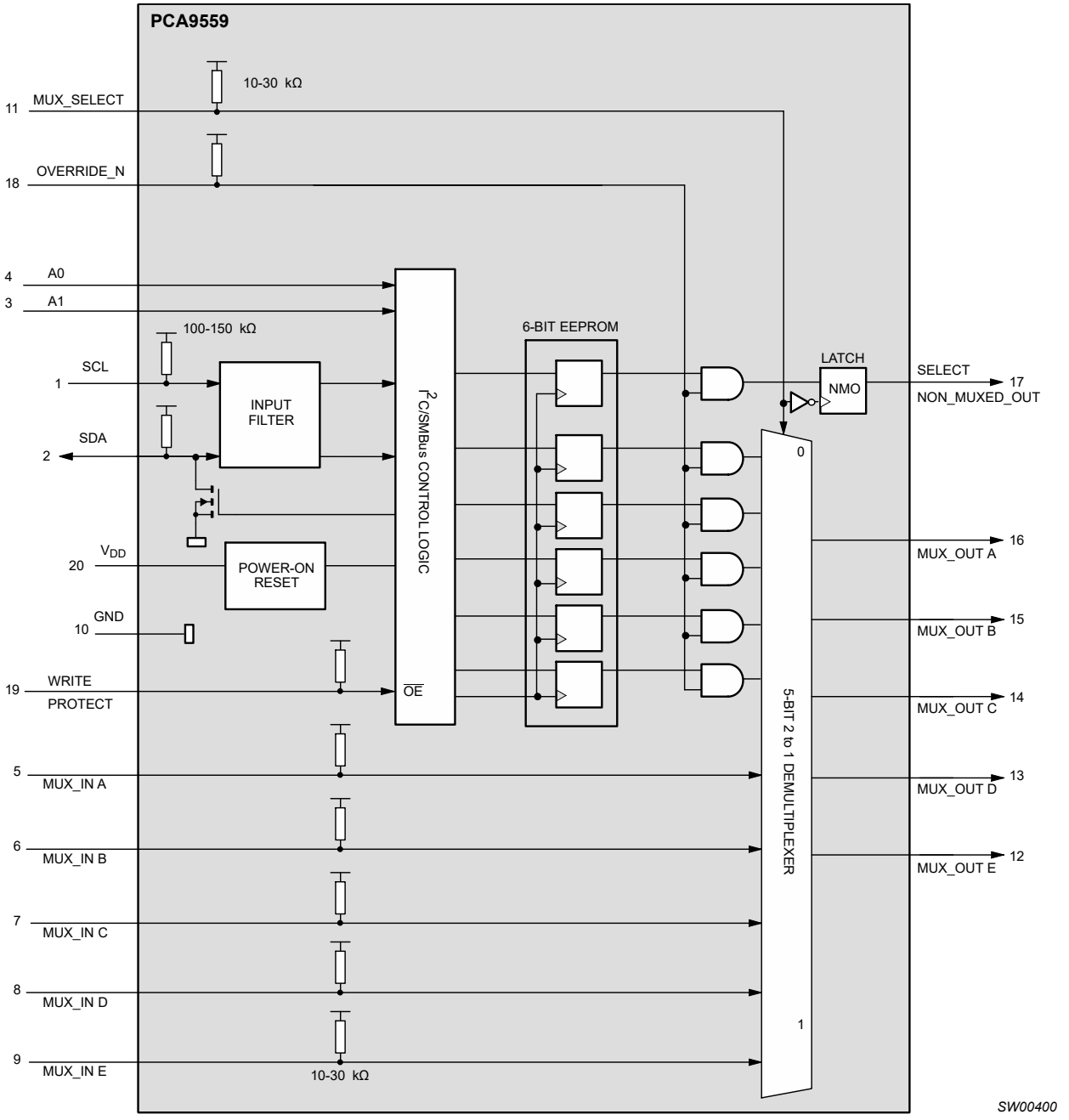


Figure 1. Block diagram of PCA9559

5 Pinning information

5.1 Pinning

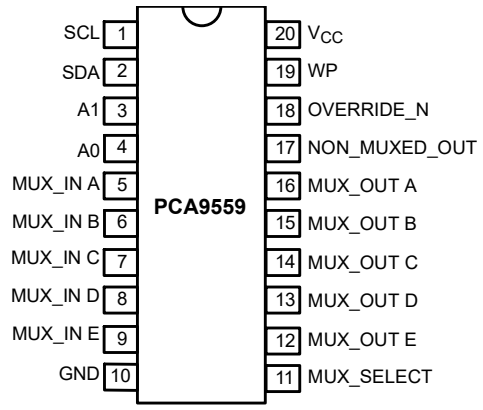


Figure 2. Pin configuration for TSSOP20

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SCL	1	serial I²C-bus clock line
SDA	2	serial bidirectional I²C-bus data line
A1	3	address 1
A0	4	address 0
MUX_IN_A	5	external input A to multiplexer
MUX_IN_B	6	external input B to multiplexer
MUX_IN_C	7	external input C to multiplexer
MUX_IN_D	8	external input D to multiplexer
MUX_IN_E	9	external input E to multiplexer
GND	10	ground
MUX_SELECT	11	selects MUX_IN inputs or register contents for MUX_OUT outputs
MUX_OUT_E	12	open-drain multiplexed output E
MUX_OUT_D	13	open-drain multiplexed output D
MUX_OUT_C	14	open-drain multiplexed output C
MUX_OUT_B	15	open-drain multiplexed output B
MUX_OUT_A	16	open-drain multiplexed output A
NON-MUXED_OUT	17	open-drain output from non-volatile memory
OVERRIDE_N	18	forces all outputs to logic 0
WP	19	non-volatile register write-protect
V_{CC}	20	supply voltage (3.0 V to 3.6 V)

6 Functional description

When the MUX_SELECT signal is logic 0, the multiplexer will select the data from the non-volatile register to drive on the MUX_OUT pins. When the MUX_SELECT signal is logic 1, the multiplexer will select the MUX_IN lines to drive on the MUX_OUT pins. The MUX_SELECT signal is also used to latch the NON_MUXED_OUT signal which outputs data from the non-volatile register. The NON_MUXED_OUT signal latch is transparent when MUX_SELECT is in a logic 0 state, and will latch data when MUX_SELECT is in a logic 1 state. When the active-LOW OVERRIDE_N signal is set to logic 0 and the MUX_SELECT signal is at a logic 0, all outputs will be driven to logic 0. This information is summarized in Table 4.

The Write Protect (WP) input is used to control the ability to write the contents of the 6-bit non-volatile register. If the WP signal is logic 0, the I²C-bus will be able to write the contents of the non-volatile register. If the WP signal is logic 1, data will not be allowed to be written into the non-volatile register.

The factory default for the contents of the non-volatile register are all logic 0. These stored values can be read or written using the I²C-bus (described in Section 6.1).

The OVERRIDE_N, WP, MUX_IN, and MUX_SELECT signals have internal pull-up resistors. See Section 11 and Section 10 for hysteresis and signal spike suppression figures.

Table 4. Function table

OVERRIDE_N	MUX_SELECT	MUX_OUT OUTPUTS	NON_MUXED_OUT OUTPUT
0	0	All 0s	All 0s
0	1	MUX_IN inputs	latched NON-MUXED_OUT [1]
1	0	From non-volatile register	From non-volatile register
1	1	MUX_IN inputs	From non-volatile register

[1] NON_MUXED_OUT state will be the value present on the output at the time of the MUX_SELECT input transitioned from a logic 0 to a logic 1 state.

6.1 I²C-bus interface

Communicating with this device is initiated by sending a valid address on the I²C-bus. The address format has 5 fixed bits and two user-programmable bits followed by a 1-bit read/write value which determines the direction of the data transfer.

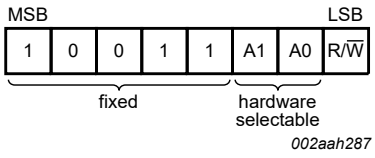


Figure 3. I²C address byte

Following the address and acknowledge bit are 8 data bits which, depending on the read/write bit in the address, will read data from or write data to the non-volatile register. Data will be written to the register if the read/write bit is logic 0 and the WP input is logic 0.

Data will be read from the register if the bit is logic 1. The four high-order bits are latched outputs, while the four low order bits are multiplexed outputs (Figure 4).

NOTE: To ensure data integrity, the non-volatile register must be internally write protected when V_{CC} to the I²C-bus is powered down or VCC to the component is dropped below normal operating levels.

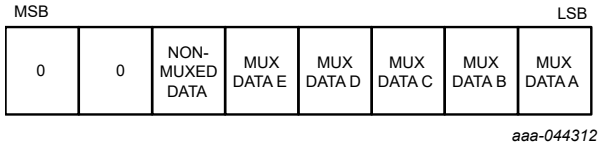


Figure 4. I²C data byte

6.2 Power-on reset

When power is applied to V_{CC}, an internal Power-On Reset (POR) holds the PCA9559 in a reset state until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9559 volatile registers and I²C/SMBus state machine will initialize to their default states.

The MUX_OUT and NON_MUXED_OUT pin values depend on:

- The OVERRIDE # and MUX_SELECT logic levels
- The previously stored values in the EEPROM registers/current MUX_IN pin values as shown in Table 1.

7 Limiting values

Table 5. Limiting values [1] [2]

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage	[3]		-1.5	V_{CC} + 1.5	V
V_O	output voltage	[3]		-0.5	V_{CC} + 1.5	V
T_{stg}	storage temperature			-60	+150	°C

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
[3] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8 Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			3.0	3.6	V
V_{IL}	LOW-level input voltage	SCL, SDA; I_{OL} = 3 mA		-0.5	+0.9	V

Table 6. Operating conditions*...continued*

Symbol	Parameter	Conditions		Min	Max	Unit
V_{IH}	HIGH-level input voltage	SCL, SDA; I_{OL} = 3 mA		2.7	4.0	V
V_{OL}	LOW-level output voltage	SCL, SDA				
		I_{OL} = 3 mA		-	0.4	V
		I_{OL} = 6 mA		-	0.6	V
V_{IL}	LOW-level input voltage	OVERRIDE_N, MUX_IN, MUX_SELECT		-0.5	+0.8	V
V_{IH}	HIGH-level input voltage	OVERRIDE_N, MUX_IN, MUX_SELECT		2.0	4.0	V
I_{OL}	LOW-level output current	MUX_OUT, NON_MUXED_OUT		-	8	mA
I_{OH}	HIGH-level output current	MUX_OUT, NON_MUXED_OUT		-	100	µA
Δt/ΔV	input transition rise and fall rate			0	10	ns/V
T_{amb}	ambient temperature			0	70	°C

9 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	TSSOP20 package		146	°C/W

10 Static characteristics

Table 8. Static characteristics

V_{HYS} is the hysteresis of Schmitt-Trigger inputs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{CC}	supply voltage			3	-	3.8	V
I_{DD}	supply current	operating mode					
		all inputs = 0 V		-	-	10	mA
		all inputs = V_{CC}		-	-	600	µA
V_{POR}	power-on reset voltage	no load; V_I = V_{CC} or GND		-	1.9	2.6	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			-0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2	-	V_{CC} = 0.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
		V_{OL} = 0.6 V		6	-	-	mA
I_{LIH}	HIGH-level input leakage current	V_I = V_{CC}		-1.5	-	-12	µA
I_{LIL}	LOW-level input leakage current	V_I = GND		-7	-	-32	µA

Table 8. Static characteristics...*continued*

V_{HYS} is the hysteresis of Schmitt-Trigger inputs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_i	input capacitance			-	-	10	pF
OVERRIDE_N, WP, MUX_SELECT							
I_{LIH}	HIGH-level input leakage current	$V_I = V_{CC}$		-20	-	-100	µA
I_{LIL}	LOW-level input leakage current	V_I = GND		-86	-	-267	µA
C_i	input capacitance			-	-	10	pF
MUX_IN_A, MUX_IN_B, MUX_IN_C, MUX_IN_D, MUX_IN_E							
I_{LIH}	HIGH-level input leakage current	$V_I = V_{CC}$		-0.166	-	-0.75	mA
I_{LIL}	LOW-level input leakage current	V_I = GND		-0.72	-	-2	mA
C_i	input capacitance			-		10	pF
Inputs A0, A1							
I_{LIH}	HIGH-level input leakage current	$V_I = V_{CC}$		-1	-	+1	µA
I_{IL}	LOW-level input current	V_I = GND		-1	-	+1	µA
C_i	input capacitance			-	-	10	pF
MUX_OUT E ⇒ A							
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA		-	-	0.4	V
		I_{OL} = 2 mA		-	-	0.7	V
NON-MUX_OUT							
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA		-	-	0.4	V
		I_{OL} = 2 mA		-	-	0.7	V

11 Dynamic characteristics

Table 9. Dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
MUX_IN ⇒ MUX_OUT							
t_{PLH}	LOW to HIGH propagation delay			-	28	37	ns
t_{PHL}	HIGH to LOW propagation delay			-	16	21	ns
Select ⇒ MUX_OUT							
t_{PLH}	LOW to HIGH propagation delay			-	30	39	ns
t_{PHL}	HIGH to LOW propagation delay			-	17	22	ns
OVERRIDE_N ⇒ NON-MUX_OUT							
t_{PLH}	LOW to HIGH propagation delay			-	34	43	ns
t_{PHL}	HIGH to LOW propagation delay			-	19	25	ns
OVERRIDE_N ⇒ MUX_OUT							
t_{PLH}	LOW to HIGH propagation delay			-	31	41	ns
t_{PHL}	HIGH to LOW propagation delay			-	21	27	ns

Table 9. Dynamic characteristics...*continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	output		1.0	-	3	ns/V
t_f	fall time	output		1.0	-	3	ns/V
P_F	Pull-up resistor for outputs			1.0	-	-	ns/V
C_L	load capacitance	test load on outputs		-	-	-	pF
I²C-bus							
f_{SCL}	SCL clock frequency			10	-	400	kHz
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition	After this period, the first clock pulse is generated		600	-	-	ns
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			600	-	-12	ns
$t_{SU;STA}$	set-up time for a repeated START condition			600	-	-32	ns
$t_{HD;DAT}$	data hold time			0	-	10	ns
$t_{SU;DAT}$	data set-up time			100	-	-100	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filters			0	-	50	ns
$t_{SU;STO}$	set-up time for STOP condition			600	-	10	ns
t_r	rise time of both SDA and SCL signals	10 - 400 pF bus		20	-	300	ns
t_f	fall time of both SDA and SCL signals	10 - 400 pF bus		20	-	300	ns
C_L	load capacitance	for each bus line		-	-	400	pF
t_W	write cycle time [1]			-	15	-	ms

[1] WRITE CYCLE time can only be measured indirectly during the write cycle. During this time, the device will not acknowledge its I²C Address.

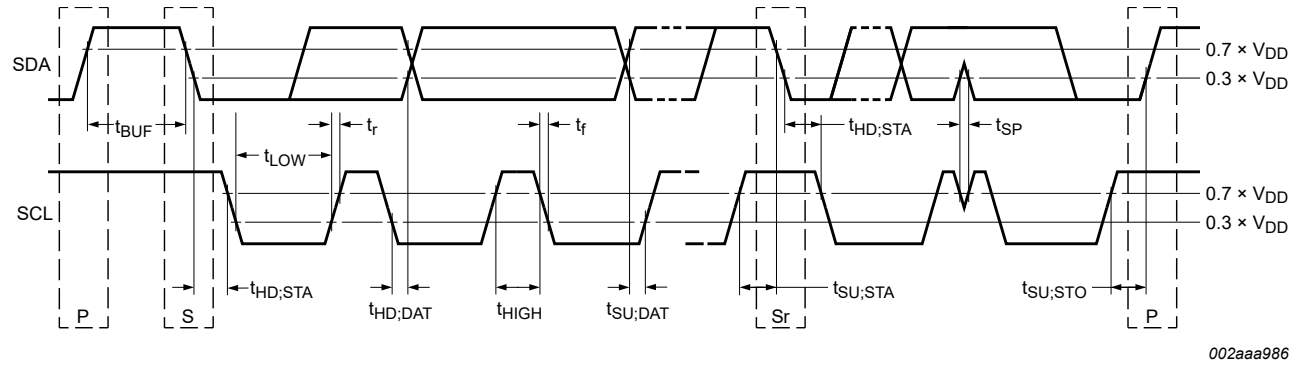


Figure 5. Definition of timing

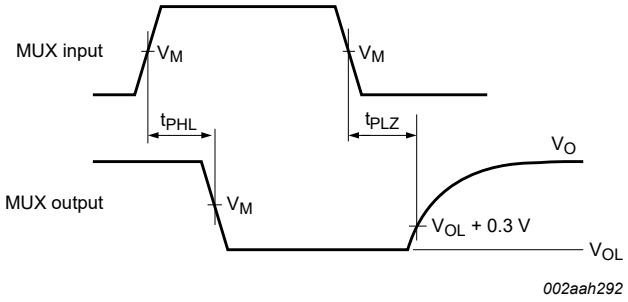


Figure 6. Open-drain output enable and disable times

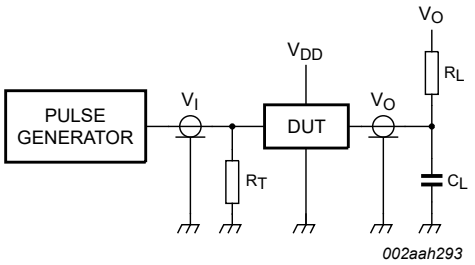
12 Non-volatile storage specifications

Table 10. Non-volatile storage specifications

Parameter	Specification
memory cell data retention	10 years (minimum)
number of memory cell write cycles	100,000 cycles (minimum)

Application note *AN250, "I²C DIP Switch"* provides additional information on memory cell data retention and the minimum number of write cycles.

13 Test information



R_L = load resistor; 1 kΩ.

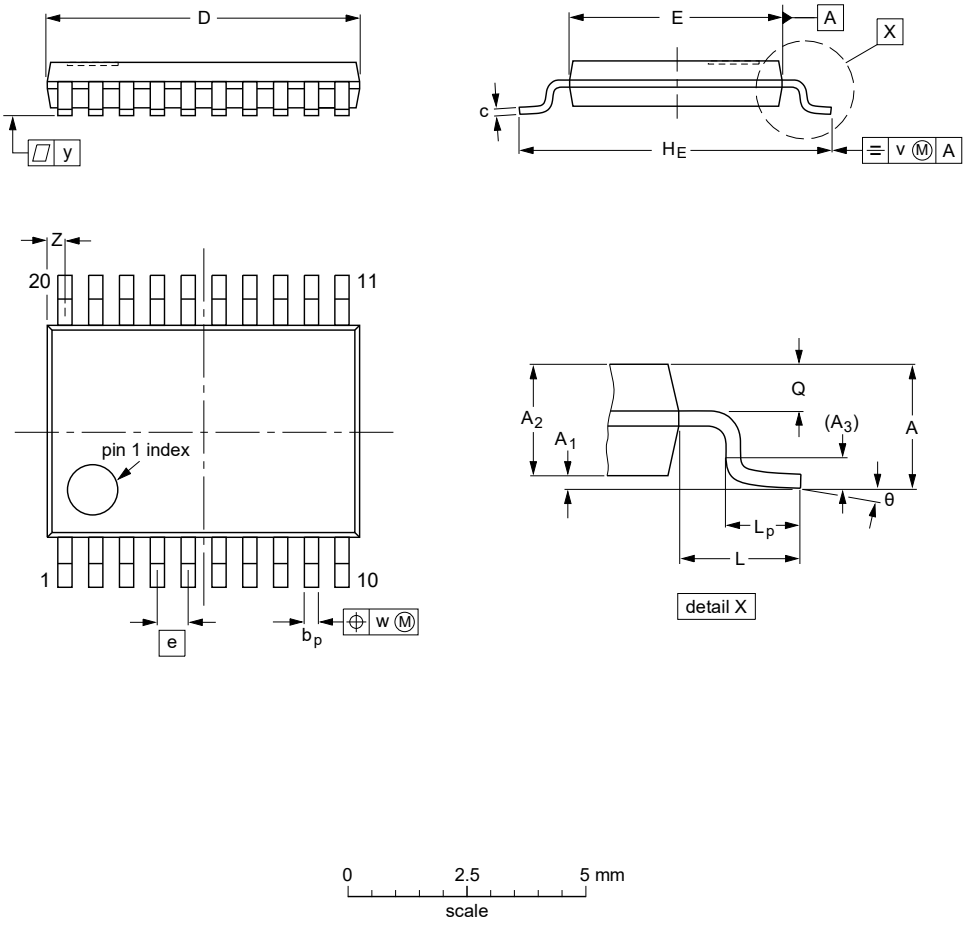
C_L = load capacitance; includes jig and probe capacitance; 10 pF.

R_T = termination resistance; should be equal to Z_o of pulse generators.

Figure 7. Test circuit for open-drain outputs

14 Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Figure 8. Package outline SOT360-1 (TSSOP20)

15 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 9) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and Table 12

Table 11. SnPb eutectic process (from J-STD-020D)

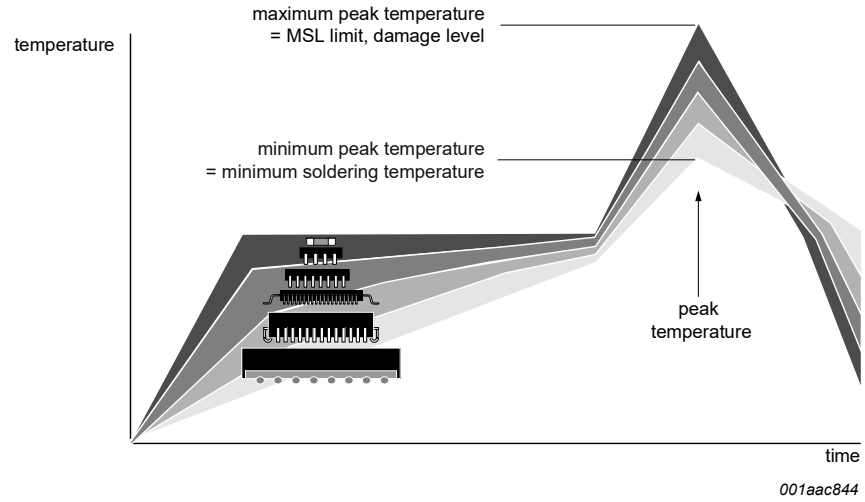
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 9.



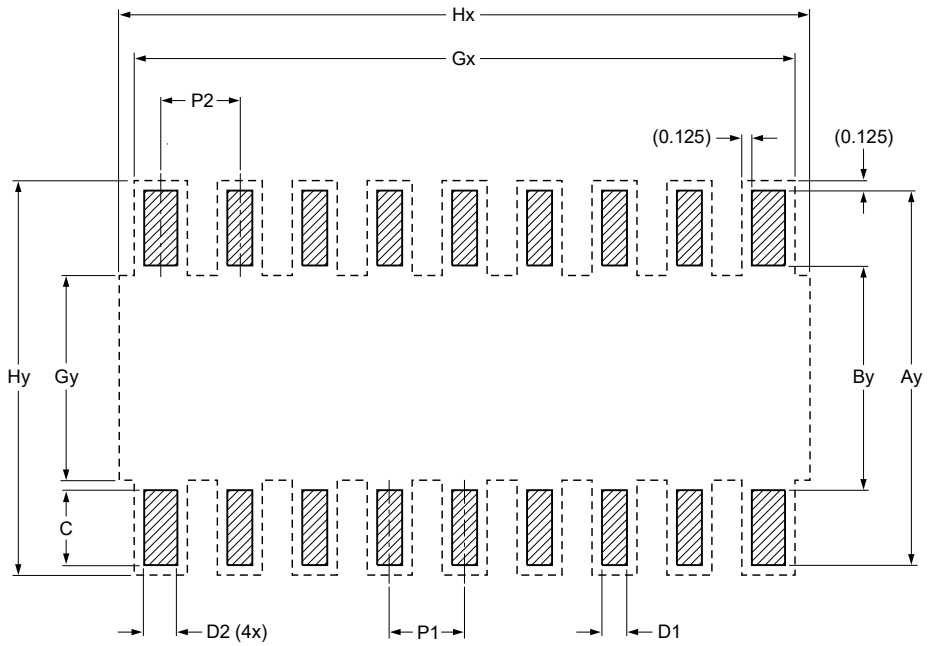
MSL: Moisture Sensitivity Level

Figure 9. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16 Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP20 package **SOT360-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	6.900	5.300	7.300	7.450

sot360-1_fr

Figure 10. PCB footprint for SOT360-1 (TSSOP20); reflow soldering

17 Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
PCB	Printed-Circuit Board
SMBus	System Management Bus
VID	Voltage IDentification code
VRM	Voltage Regulator Module

18 Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9559 v.5	20211025	Product data sheet	-	PCA9559 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Section 2: MM is removed from data sheet during update as no longer required. • Removed PCA9959PW,112; tube pack method was discontinued DN86 July 2017.			
PCA9559 v.4	20030627	Product data sheet	-	PCA9559 v.3

19 Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

19.2 Definitions

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