FAIRCHILD SEMICONDUCTOR®

August 2012

FXLA2203
Dual-Mode, Dual-SIM-Card Level Translator

Features

- Easy-to-Use “Single Pin” SIM Card Swap Control
- Channel Swap Time: 130ns (Typical)
- Simultaneous Dual-Mode, Dual-SIM Communication
- Host Ports: 1.65V to 3.6V Voltage Translation
- Card Ports: 1.65V to 3.6V Voltage Translation
- Leverages the Presence of Existing PMIC LDOs
- ISO7816 Compliant
- Power Switch R_{ON}: 0.5Ω (Typical)
- Supports Class B 3V SIM / UIM Cards
- Supports Class C: 1.8V SIM / UIM Cards
- Non-Preferential Host V_{CC} Power-Up Sequencing
- Activation / Deactivation Timing Compliant per ISO7816-03
- Internal Pull up Resistors for Bi-Directional I/O Pin
- Outputs Switch to 3-State if Host V_{CC} at GND
- Power-Off Protection
- Packaged in 24-Terminal UMLP (2.5mm x 3.5mm)
- Direction Control Not Needed

Applications

- Dual-Mode Dual-SIM Applications
- GSM, CDMA, WCDMA, TDSCDMA CDMA2000, 3G Cellular Phones
- Mobile TV: OMA BCAST

Description

The FXLA2203 allows either two hosts to simultaneously communicate with two Subscriber Identity Modules (SIM), or two User Identity Modules (UIM). Dual Mode refers to the mobile phones that are compatible with more than one form of data transmission or network (such as GSM, CDMA, WCDMA, TDSCDMA, or CDMA2000), resulting in a dual-baseband processor configuration. In a dual-mode application, the FXLA2203 host ports interface directly with the baseband processors *(see Figure 9)*.

The bi-directional I/O open-drain channel features auto-direction and internal 10KΩ pull-up resistors. RST and CLK provide unidirectional translation from host to card only.

Either host can swap SIM slots with the assertion of a single control pin: CH_Swap. The typical channel swap time is 130ns.

The FXLA2203 does not contain internal Low Dropout Regulator (LDOs). Instead, the FXLA2203 architecture incorporates two low-R_{ON} internal power switches for routing existing PMIC (Power Management Integrated Circuit) LDOs to individual SIM slots. This reduces overall system power, leverages existing LDO system resources, and aligns with the philosophy that centralizing LDOs in the PMIC facilitates power management. Since the FXLA2203 does not block the LDO function to the SIM card, existing activation / deactivation timing transparency is maintained between Hosts, PMICs, and SIM cards.

The device allows voltage translation from as high as 3.6V to as low as 1.65V. Each port tracks its own port power supply.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FXLA2203UMX	-40 to 85°C	24-Terminal, 2.5mm x 3.4mm Ultrathin Molded Leadless Package (UMLP), 0.4mm Pitch	Tape and Reel

Block Diagram

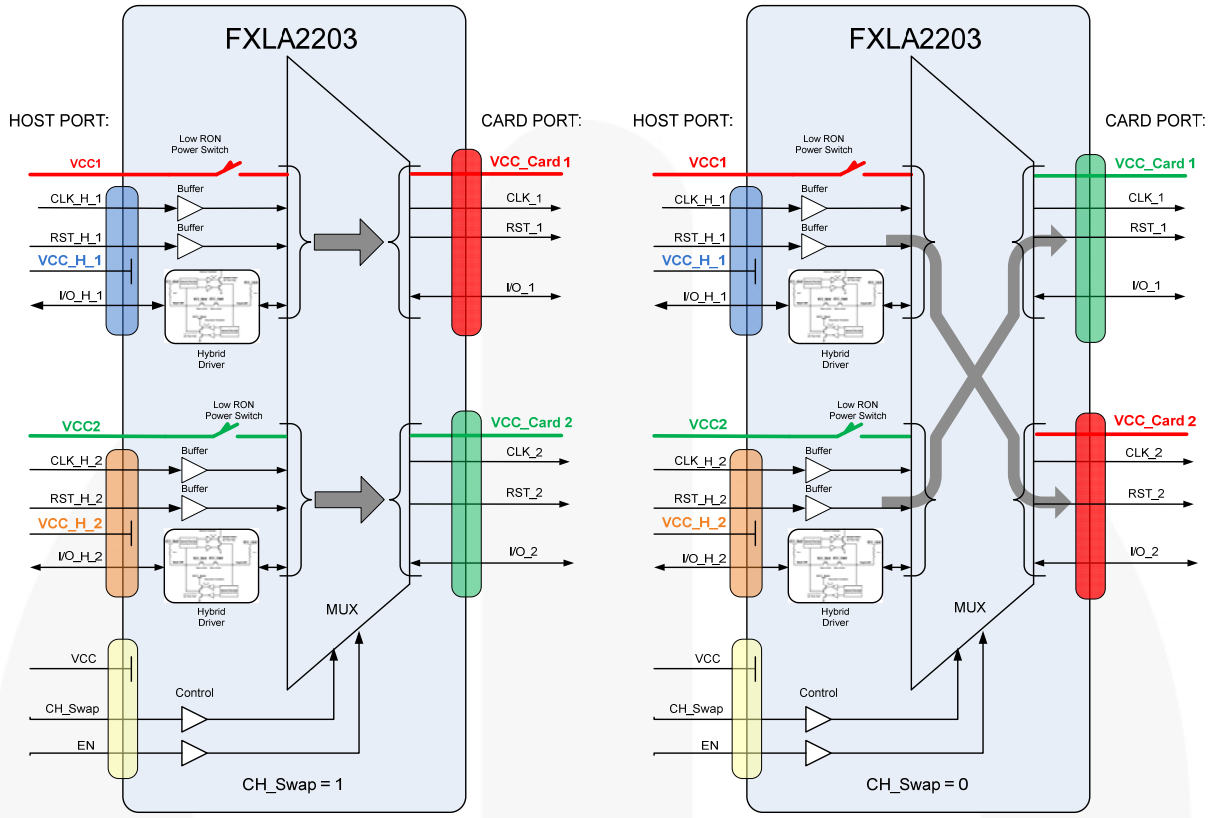


Figure 1. Block Diagram

Notes:

1. V_{CC} must always be greater than or equal to (≥) V_{CC1} and V_{CC2}.
2. Hybrid driver explained in detail in Figure 12 - I/O Pin Functional Diagram.
3. *See Table 2 for CH_Swap truth table*.

Pin Configuration

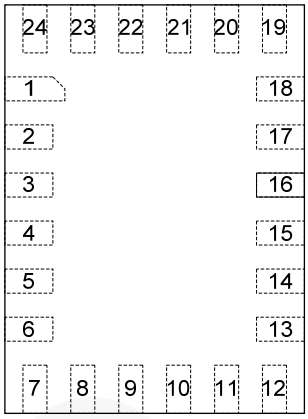


Figure 2. Top Through View

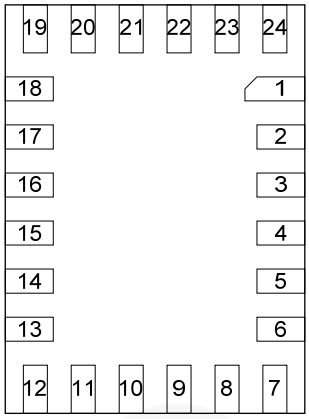


Figure 3. Bottom View

Pin Definitions

Pin #	Name	Signal	Description
1	NC	NC	No Connection
2	VCC1	I	Power Supply 1 Input: Coming from PMIC 1 LDO
3	VCC_Card1	O	Power Output for Card Slot 1
4	GND	GND	Ground
5	VCC_Card2	O	Power Output for Card Slot 2
6	VCC2	I	Power Supply 2 Input: Coming from PMIC 2 LDO
7	RST_2	O	Reset Output to Card Slot 2
8	I/O_2	I/O	Data I/O for Card Slot 2; Open Drain
9	CLK_2	O	Clock Output to Card Slot 2
10	CLK_H_2	I	Clock Input of Host Interface 2
11	RST_H_2	I	Reset Input of Host Interface 2
12	I/O_H_2	I	Data I/O of Host Interface 2; Open Drain
13	VCC_H_2	Supply	Power Supply of Host Interface 2
14	GND	GND	Ground
15	V_{CC}	Supply	Power Supply of Control Pins: EN and CH_Swap
16	EN	I	GPIO Enable. LOW disables both SIM card slots. HIGH enables both SIM card slots. Connect to V_{CC} if not used. Default level after power up is LOW.
17	Ch_Swap	I	Channel Swap. “1” host 1 to card slot 1, host 2 to card slot 2. “0” host 1 to card slot 2, host 2 to card slot 1. Connected to V_{CC} if not used. Default level after power up is LOW.
18	VCC_H_1	Supply	Power Supply of Host Interface 1
19	I/O_H_1	I/O	Data I/O of Host Interface 1; Open Drain
20	RST_H_1	I	Reset Input of Host Interface 1
21	CLK_H_1	I	Clock Input of Host Interface 1
22	CLK_1	O	Clock Output to Card Slot 1
23	I/O_1	I/O	Data I/O for Card Slot 1; Open Drain
24	RST_1	O	Reset Output to Card Slot 1

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage		V_{CC}	-0.5	5.0	V
			VCC_H_n, VCCn	-0.5	4.6	V
V_{IN}	DC Input Voltage		Host Ports and Card Ports	-0.5	4.6	V
			Control Input (EN and CH_Swap)	-0.5	5.0	
V_O	Output Voltage[4]		Output 3-State	-0.5	4.6	V
			Output Active (Host Port)	-0.5	V_{CC} +0.5	
			Output Active (Card Port)	-0.5	V_{CC} +0.5	
I_{IK}	DC Input Diode Current		V_I<0V		-50	mA
I_{OK}	DC Output Diode Current		V_O<0V		-50	mA
			V_O>V_{CC}		+50	
I_{OH}/I_{OL}	DC Output Source / Sink Current[4]			-50	+50	mA
I_{CC}	DC V_{CC} or Ground Current (per Supply Pin)				±100	mA
T_{STG}	Storage Temperature Range			-65	+150	°C
P_{DISS}	Power Dissipation at 5MHz				0.57	W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114[5]	Card Side Pins 3-5, 7-9, 14, 22-24		9	kV
			All Other Pins		3	
		Charged Device Model, JESD22-C101	Card Side Pins 3-5, 7-9, 14, 22-24		2	
			All Other Pins		2	

Notes:

4. I_O absolute maximum ratings must be observed.
5. Human Body Model (HBM): R=1500Ω, C=100pF.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Power Supply[6]	V_{CC}	1.65	4.35	V
		VCC_H_n, VCCn	1.65	3.60	V
V_{IN}	Input Voltage[7]	Host Port	0	3.6	V
		Card Port	0	3.6	V
V_{OUT}	Output Voltage[7]	Host Port	0	3.6	V
		Card Port	0	3.6	V
		Host Port I/O Pin	0	VCC_H_n +0.3V	V
		Card Port I/O Pin	0	VCCn +0.3V	V
T_A	Operating Temperature, Free Air		-40	+85	°C
dt/dV	Input Edge Rate	RST and CLK		10	ns/V
Θ_{JA}	Junction-to-Ambient Thermal Resistance			52.1	C/W

Notes:

6. V_{CC} must always be equal to, or greater than, V_{CC1} and V_{CC2}.
7. All unused inputs and input/outputs must be held at their respective V_{CC} or GND.

DC Electrical Characteristics

T_A=-40°C to +85°C; pins I/O_1, I/O_2, I/O_H_1, I/O_H_2 (open drain).

Symbol	Parameter	Conditions	$V_{CC\_H\_n}$ (V)	V_{CCn} (V)	Min.	Typ.	Max.	Unit
V_{IH_host}	High-Level Input Voltage	Data Inputs of Host Interface	1.65 – 3.60	1.65 - 3.60	0.7 x $V_{CC\_H\_n}$			V
V_{IH_card}		Data Inputs of Card Interface	1.65 – 3.60	1.65 - 3.60	0.7 x V_{CCn}			V
V_{IL_host}	Low-Level Input Voltage	Data Inputs of Host Interface	1.65 – 3.60	1.65 - 3.60			0.4	V
V_{IL_card}		Data Input of Card Interface	1.65 – 3.60	1.65 - 3.60			0.15 x V_{CCn}	V
V_{OH_host}	High-Level Output Voltage	I_{OH}=-20µA	1.65 – 3.60	1.65 - 3.60	0.7 x $V_{CC\_H\_n}$			V
V_{OH_card}		I_{OH}=-20µA	1.65 – 3.60	1.65 - 3.60	0.7 x V_{CCn}			V
V_{OL_host}	Low-Level Output Voltage	I_{OL}=1mA, V_{IL}=0V	1.65 – 3.60	1.65 - 3.60			0.05	V
V_{OL_card}		I_{OL}=1mA, V_{IL}=0V	1.65 – 3.60	1.65 - 3.60			0.05	V
V_{OL_host}	Low-Level Output Voltage	I_{OL}=1mA, V_{IL}=0.100V	1.65 – 3.60	1.65 - 3.60			0.15	V
V_{OL_card}		I_{OL}=1mA, V_{IL}=0.100V	1.65 – 3.60	1.65 - 3.60			0.15	V
V_{OL_host}	Low-Level Output Voltage	I_{OL}=1mA, V_{IL}=0.250V	1.65 – 3.60	1.65 - 3.60			0.3	V
V_{OL_card}		I_{OL}=1mA, V_{IL}=0.250V	1.65 – 3.60	1.65 - 3.60			0.3	V
I_{OFF}	Power-Off Leakage Current	V_O=0V to 3.6V Host and Card Sides	3.60	0			±1.0	µA
I_{OZ}	3-State Output Leakage	V_O=0V or 3.6V, EN=GND, Host and Card Sides	3.60	3.60			±1.0	µA
I_{OZ}	3-State Output Leakage	V_O=0V or 3.6V, EN=1, Host and Card Sides	0	3.60			±1.0	µA
R_{pull_up}	Internal Pull-Up Resistor		1.65 – 3.60	1.65 - 3.60	9	10	11	KΩ

DC Electrical Characteristics

T_A=-40°C to +85°C; pins EN, CH_Swap.

Symbol	Parameter	Conditions	V_{CC} (V)	Min.	Max.	Unit
V_{IL}	Low-Level Input Voltage		3.60		0.65	V
			1.80		0.45	V
V_{IH}	High-Level Input Voltage		3.60	1.2		V
			1.80	0.9		V
I_L	Input Leakage Current	V_I=V_{CC} or GND, I/O Floating	1.65 – 3.60		±1	µA
I_{CCT}	Increase in I_{CC} per Pin	V_{IN}=1.8V	3.60		12	µA
		V_{IN}=0.9V	1.80		10	µA

DC Electrical Characteristics

T_A=-40°C to +85°C; pins RST_1, RST_2, RST_H_1, RST_H_2, CLK_1, CLK_2, CLK_H_1, CLK_H_2.

Symbol	Parameter	Conditions	$V_{CC\_H\_n}$ (V)	V_{CCn} (V)	Min.	Typ.	Max.	Unit
V_{IL}	Low-Level Input Voltage		1.65 – 3.60	1.65 – 3.60			0.35 x $V_{CC\_H\_n}$	V
V_{IH}	High-Level Input Voltage		1.65 – 3.60	1.65 – 3.60	0.65 x $V_{CC\_H\_n}$			V
V_{OL}	Low-Level Output Voltage	I_{OL}=20µA	1.65 – 3.60	1.65 – 3.60			0.12 x V_{CCn}	V
V_{OH}	High-Level Output Voltage	I_{OH}=-20µA	1.65 – 3.60	1.65 – 3.60	0.80 x V_{CCn}			V
I_I	Input Leakage Current	V_I=V_{CC} or GND	1.65 – 3.60	3.60			±1	µA
I_{OFF}	Power-Off Leakage Current	V_O=0V to 3.6V	3.60	0			±1	µA
I_{OZ}	3-State Output Leakage	V_O=0V or 3.6V, EN=GND	3.60	3.60			±1	µA
		V_O=0V or 3.6V, EN=1	0	3.60			±1	
I_{CC}	Quiescent Supply Current	V_I=V_{CC} or GND; I_O=0, EN=V_{CC}, I/O Floating	1.65 – 3.60	1.65 – 3.60			3	µA
I_{CCZ}	Power-Down Supply Current	V_I=V_{CC} or GND; I_O=0, EN=GND	1.65 – 3.60	1.65 – 3.60			3	µA
R_{ONPS}	Power Switch On Resistance, EN=1	I_{ON}=50mA, VCCn to VCC_Cardn	1.65 – 3.60	1.65 – 3.60		0.5	0.8	Ω
R_{OFPS}	Power Switch OFF Resistance, EN=0	CH_Swap=0 and 1, $V_{CC1/2}$=3.3V	1.65 – 3.60	1.80 – 3.60		50		MΩ

AC Characteristics

Card Port (RST, CLK)

Unless otherwise specified, output load: C_L=30pF, $R_L \geq 1M\Omega$; T_A=-40°C to +85°C; V_{CCn}=1.65V to 3.60V.

Symbol	Parameter	Typ.	Max.	Unit
t_r	Output Rise Time Card Port(8,10)	1	5	ns
t_f	Output Fall Time Card Port(9,10)	1	5	ns

Notes:
8. *See Figure 6*.
9. *See Figure 7*.
10. t_r, t_f guaranteed by characterization; not production tested.

Host and Card Port (I/O Only)

Unless otherwise specified, output load: C_L=30pF, $R_L \geq 1M\Omega$, and open-drain outputs; T_A=-40°C to +85°C; V_{CCn}=1.65V to 3.60V; and $V_{CC\_H\_n}$=1.65V to 3.60V.

Symbol	Conditions	Parameter	Typ.	Max.	Unit
t_r(11,13)	Open Drain Inputs with 500µA I_{SINK}(13)	Output Rise Time Card Port (10% - 90%)	200	500	ns
t_f(12,13)		Output Fall Time Card Port (90% - 10%)	2.5	4.0	ns
t_r(11,13)		Output Rise Time Host Port (10% - 90%)	200	500	ns
t_f(12,13)		Output Fall Time Host Port (90% - 10%)	2	3	ns

Notes:
11. *See Figure 6*.
12. *See Figure 7*.
13. t_r, t_f guaranteed by characterization; not production tested.

$V_{CC\_H\_n}$=1.65V to 3.60V(16)

Unless otherwise specified, T_A=-40°C to +85°C and V_{CCn}=1.65V to 3.60V.

Symbol	CH_Swap	Direction	Path	Typ.	Max.	Unit
t_{swap}	HL, LH	Host → Card	RST, CLK, I/O and Power Switches	130	400	ns

Notes:
14.
15.
16. The power switch swap time assumes no decoupling capacitors on the VCC_Card pins.
17. t_{swap} is the time required for the CH_Swap pin to swap host to SIM slot connections.
18. The I/O pin swap time assumes a push / pull driver; otherwise, the rise time (RC time constant) of an open-drain driver masks the actual I/O pin switch time.

Maximum Frequency(19)

Unless otherwise specified, CLK (Host to Card), T_A=-40°C to +85°C, and card port V_{CCn}=1.65V to 3.60V.

Host Port: $V_{CC\_H\_n}$	CH_Swap	Minimum	Unit
1.6V to 3.6V	1	30	MHz
	0	30	

Note:
19. Maximum frequency is guaranteed but not tested.

Power Dissipation Capacitance

T_A=+25°C.

Symbol	Parameter	Conditions	Typical	Unit
C_{pd}	Power Dissipation Capacitance	$V_{CC\_H\_n}$=V_{CCn}=V_{CC}=3.3V, V_I=0V or V_{CC}, CH_Swap=1, CLK1 and CLK2 Switching at 5MHz	23	pF

Test Diagrams

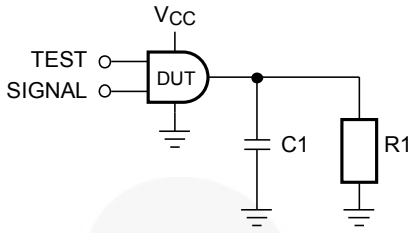


Figure 4. Test Circuit

Table 1. AC Test Conditions

V_{CCO}	C1	R1
1.8V± 0.15V	30pF	1MΩ
2.5V ± 0.2V	30pF	1MΩ
3.3 ± 0.3V	30pF	1MΩ

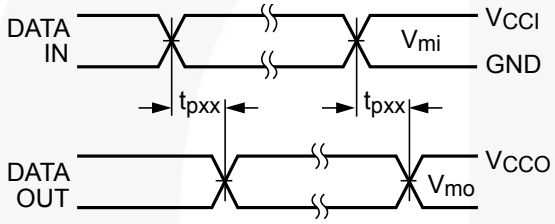


Figure 5. Input Edge Rates for RST and CLK

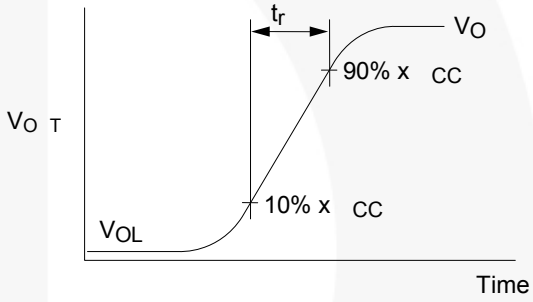


Figure 6. Active Output Rise Time

Notes:
20. Input $t_R=t_F$=2.0ns, 10% to 90% at V_I=2.5V.
21. Input $t_R=t_F$=2.5ns, 10% to 90% at V_I=2.5V.

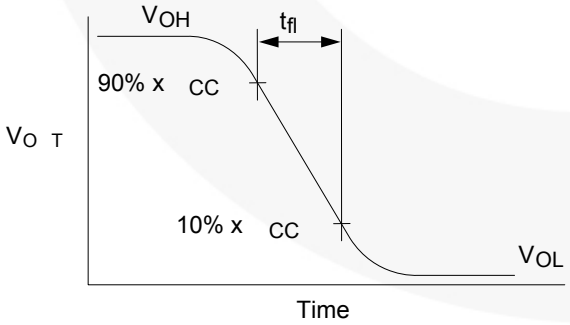


Figure 7. Active Output Fall Time

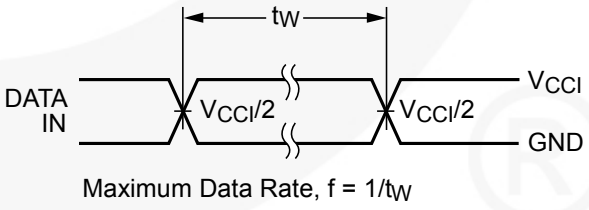


Figure 8. Maximum Data Rate

Application Information

Figure 9 illustrates an FXLA2203 used in a dual-mode / dual-SIM application. The FXLA2203 does not contain any internal LDOs. Instead, the FXLA2203 architecture incorporates two low-R_{ON} internal power switches for routing existing Power Management Integrated Circuit (PMIC) LDOs to individual SIM slot VCC pins.

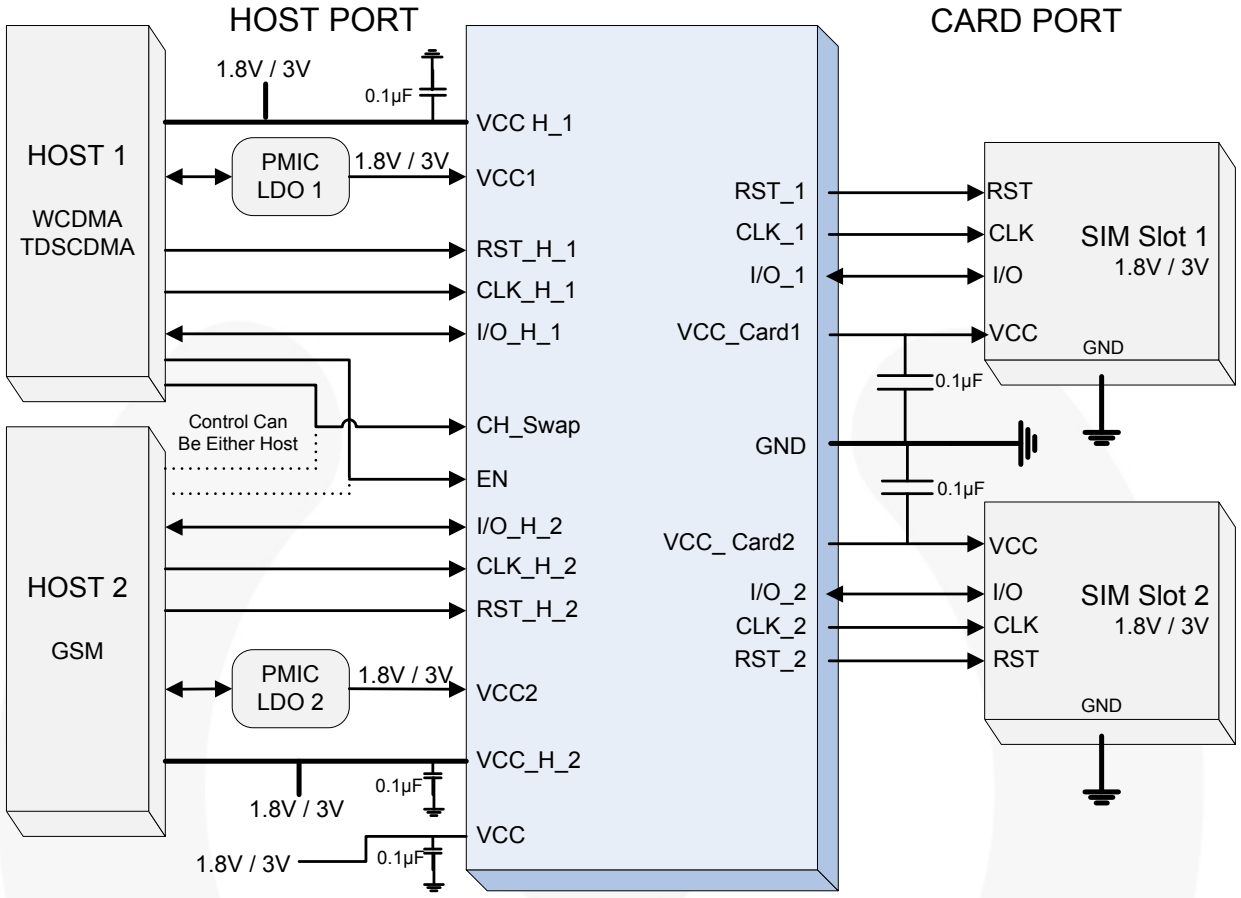


Figure 9. Typical Dual-Mode Application

CH_Swap Truth Table

CH_Swap controls simultaneous communication between Host 1 or Host 2, and either SIM Card according to Table 2 — Dual-Mode, Dual-SIM Truth Table. Either host can swap SIM slots (130ns typical) with the assertion of the CH_Swap pin. This simple solution is faster and less complicated than SPI or I^2C communication protocols.

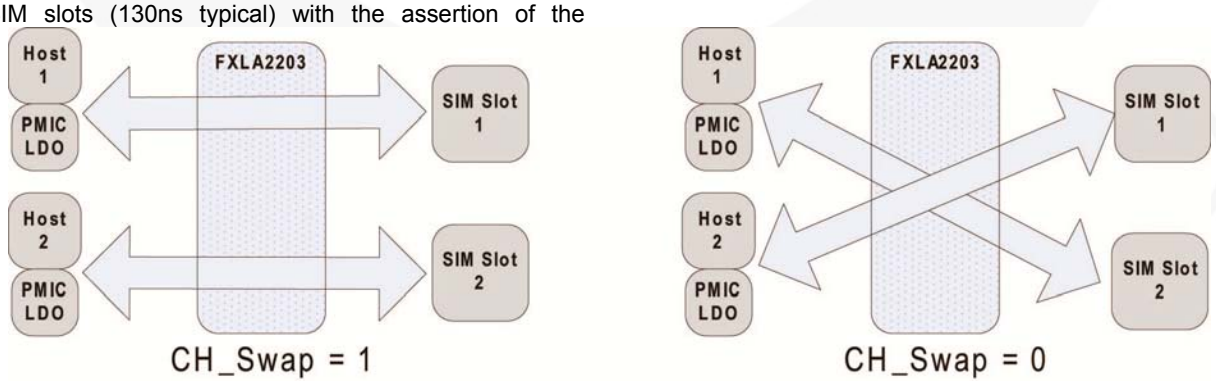


Figure 10. CH_Swap

Table 2. Dual-Mode, Dual-SIM Truth Table

Enable	CH_SWAP	Configuration
1	1	Host 1 → SIM Slot 1
1	1	Host 2 → SIM Slot 2
1	0	Host 1 → SIM Slot 2
1	0	Host 2 → SIM Slot 1

Voltage Translation Description

The FXLA2203 provides full voltage translation, or level shifting, from 1.65V – 3.6V between Host 1 or Host 2 and either SIM card (according to Table 3). The host sides reference $V_{CC\_H\_1}$ and $V_{CC\_H\_2}$, respectively, while each SIM slot references the external PMIC LDO voltage level determined by the CH_Swap pin. This architecture offers a flexible solution for problematic V_{CC} domain disagreements. For example, if Host 1 operates at 1.65V and Host 2 operates at 2.5V, while slot 1 is populated with a 3.0V SIM card and slot 2 is populated with a 1.8V SIM card, the FXLA2203 provides seamless voltage translation across all four V_{CC} domains.

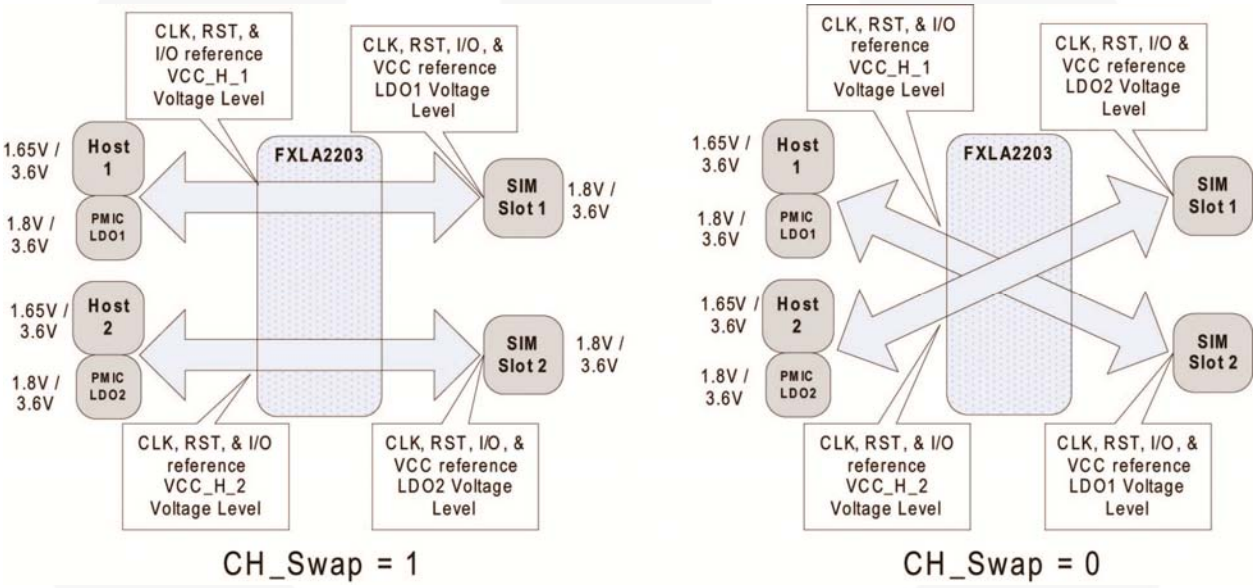


Figure 11. Voltage Translation

Table 3. Translation Truth Table

Enable	CH_Swap	SIM Slot 1 Voltage Levels	SIM Slot 2 Voltage Levels
1	1	PMIC LDO1 / V_{CC1}	PMIC LDO2 / V_{CC2}
1	0	PMIC LDO2 / V_{CC2}	PMIC LDO1 / V_{CC1}

Note:

22. V_{CC} must always be greater than or equal to (≥) V_{CC1} and V_{CC2}.

I/O Pin Function

The ISO7816-3 specification, which governs the SIM card physical layer requirements, identifies the I/O pin as a bi-directional open-drain pin. To provide auto-direction for the I/O pin, the FXLA2203 architecture (Figure 12) implements two series NpassGates and two dynamic drivers. This hybrid architecture is highly beneficial in a SIM card interface.

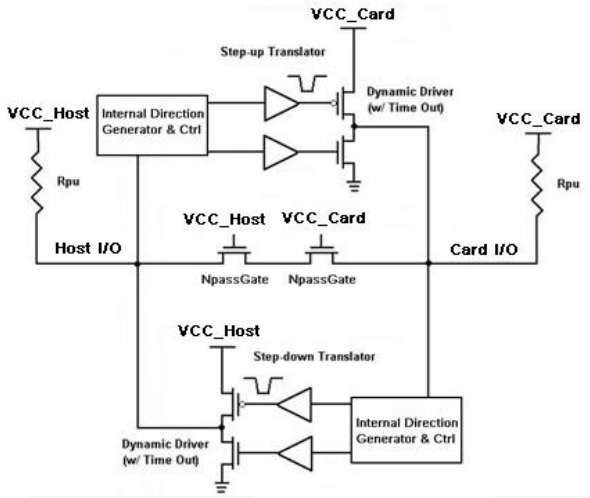


Figure 12. I/O Pin Functional Diagram

The hybrid bi-directional I/O channel contains two series NpassGates and two dynamic drivers. This architecture allows auto-direction functionality without the need for a direction pin from either the host or the SIM card and accomplishes an automatic change in direction without the presence of an edge.

Due to open-drain technology, hosts and SIM cards do not use push-pull drivers on the I/O pin. Logic LOWs are pulled down (I_{sink}), while logic HIGHs are "let go" (3-state). During a logic LOW on the I/O pin, both series NpassGates are turned on and act like a very low resistive short between the host and the SIM card. When the host or card lets go of a previously held LOW on the I/O pin, the rise time is largely determined by the RC time constant, where R is the internal pull-up resistor (10KΩ) and C is the I/O signal trace capacitance. The FXLA2203 acts as a very low resistive short between the host and SIM card (during a LOW) until either of the port's $V_{CC/2}$ thresholds are reached. After the RC time constant has reached the $V_{CC/2}$ threshold of either port, the port's edge detector triggers both dynamic drivers to drive their respective ports in the LOW-to-HIGH (LH) direction, accelerating the rising edge. The resulting rise time resembles the CH2 waveform (blue) of Figure 13. Effectively, two distinct slew rates appear in the rise time. The first slew rate (slower) is the RC time constant of the I/O signal trace. The second slew rate (faster) is the dynamic driver accelerating edge.

If both the host and card ports of the I/O pin are HIGH, a high-impedance path exists between the host and card ports because both of the series NpassGates are turned off. If a host or SIM card pulls the I/O pin LOW, that device's driver pulls down (I_{sink}) the I/O pin until the HIGH-to-LOW (HL) edge reaches the host or card port's $V_{CC/2}$ threshold. When either the host or card port threshold is reached, the port's edge detectors trigger both dynamic drivers to drive their ports in the HIGH-to-LOW (HL) direction, accelerating the falling edge.

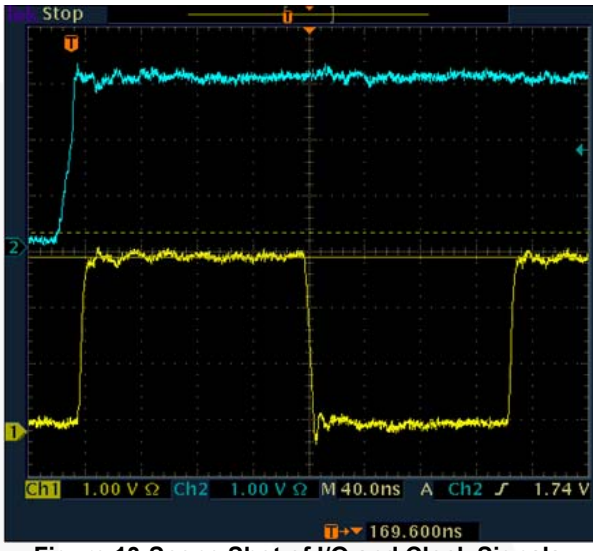


Figure 13. Scope Shot of I/O and Clock Signals CH1: CLK Pin (Yellow), CH2: I/O PIN (Blue) Driven by the FXLA2203

Activation / Deactivation

To ensure the SIM card electrical circuits do not activate before the contacts of the SIM card are mechanically connected, ISO7816-3 2006 mandates the activation sequence of events described in Figure 14. The FXLA2203 provides full transparency to the activation timing between host and SIM card.

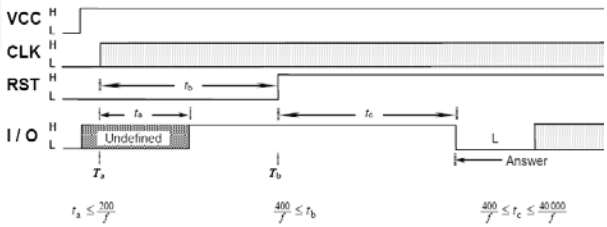


Figure 14. Activation Timing (ISO 7816-3 2006)

To ensure the SIM card electrical circuits properly deactivate before the contacts of the SIM card are mechanically connected, ISO7816-3 2006 mandates the sequence of events described in Figure 15 The FXLA2203 provides full transparency to the deactivation timing between host and SIM card.

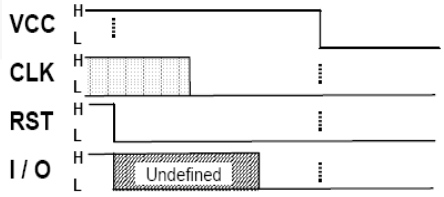


Figure 15. Deactivation (ISO 7816-3 2006)

Power-Up / Power-Down Sequence

Table 4. Power Supply Pins

Pin	Name	Function
1	VCC	EN and CH_Swap Supply
2	VCC_H_1	Host 1 Supply
3	VCC_H_2	Host 2 Supply
4	VCC1	Power Switch 1 Input
5	VCC2	Power Switch 2 Input

The V_{CC} host power sequencing is non preferential; however, V_{CC} must be higher or equal to V_{CC1} and V_{CC2}. The Enable pin must be LOW while V_{CC1} and V_{CC2} ramp up to valid supply voltages or ramp down to 0V.

A pull-up resistor tying enable to ground should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power up or power down. The size of the pull-up resistor is based upon the current sinking capability of the device driving the Enable pin.

Recommended power-up sequence *(see Figure 16)*:

1. Apply power to VCC.
2. Assert EN LOW (FXLA2203 disabled).
3. Apply power to VCC1, VCC2, VCC_H_1, and VCC_H_2.
4. Assert EN HIGH (FXLA2203 enabled).
5. Begin activation timing *(see Figure 14)*.

Recommended power-down sequence *(see Figure 17)*:

1. Complete deactivation timing *(see Figure 15)*.
2. Assert EN LOW (FXLA2203 disabled).
3. Ramp down power to VCC1, VCC2, VCC_H_1, and VCC_H_2.
4. Once VCC1 and VCC2 are OFF, ramp down VCC.

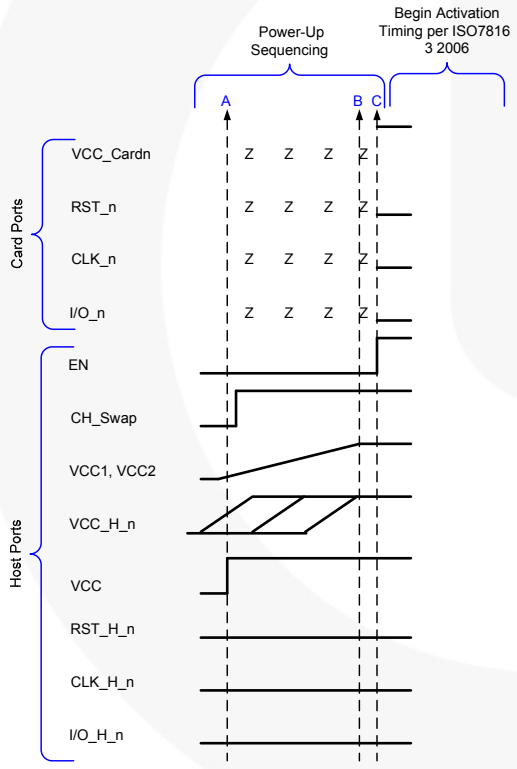


Figure 16. Power-Up Sequencing

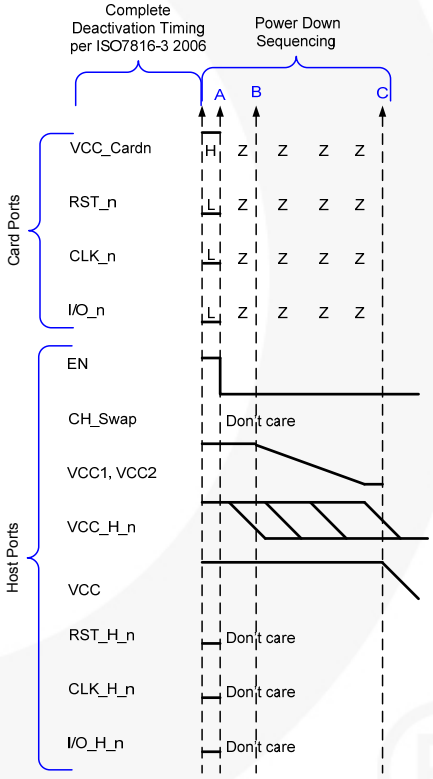


Figure 17. Power-Down Sequencing

Notes:
23. A=VCC becomes a valid voltage, EN=LOW.
24. B=VCC1, VCC2, and VCC_H_n become valid voltages, EN=LOW.
25. C=FXLA2203 enabled (EN goes HIGH), ready for activation (ISO7816-3).

Notes:
26. A=Disable FXLA2203, bring EN LOW.
27. B=Ramp down VCC1, VCC2, and VCC_H_n.
28. C=Ramp down VCC once VCC1 and VCC2 are off.

Operation Description

Table 5. Power Supply Pins

Pin	Name	Function
6	VCC	EN and CH_Swap Supply
7	VCC_H_1	Host 1 Supply
8	VCC_H_2	Host 2 Supply
9	VCC1	Power Switch 1 Input
10	VCC2	Power Switch 2 Input

The control pins EN and CH_Swap reference V_{CC}. V_{CC} can range from 1.65V to 3.6V and is independent from the other four power pins; however, V_{CC} must always be higher or equal to VCC1 and VCC2.

VCC_Host_1 and VCC_Host_2 can independently range from 1.65V to 3.6V and are the power supply pins for their respective host-side interfaces; including RST, I/O, and CLK.

VCC1 and VCC2 can independently range from 1.65V to 3.6V and are the inputs to the internal power switches. VCC1 and VCC2 should be connected to external PMIC LDOs. Depending on the logic state of the CH_Swap and EN control pins, the external LDOs are routed through the two power switches to either VCC_Card1 or VCC_Card2 *(see Table 6)*. Meanwhile, CH_Swap also routes the host (1 or 2) signal pins; RST, I/O, and CLK to the SIM Slot side (1 or 2). *See section "SIM Slot Signals: Active vs. 3-State" for details.* The voltage reference of each SIM slot is determined by the LDO voltage assigned to that SIM slot.

RST and CLK are unidirectional pins always going in the SIM slot direction. I/O is a bi-directional, open drain pin. Internal 10KΩ pull-up resistors are provided.

The ISO7816 standard identifies an algorithm that allows a Host device to auto-detect the operating voltage of a SIM card. The algorithm is called "class selection" and the FXLA2203 is 100% transparent to class selection.

If VCC1 and VCC_H_1 share the same voltage potential; these two pins can be tied together. Likewise, if VCC2 and VCC_H_2 share the same voltage potential, these two pins can be tied together. Under these conditions, and once CH_Swap has been established, the host can power up or down the SIM card along with the FXLA2203 host side solely by the LDO voltage. This feature is a convenient method for conserving power. Note that V_{CC} must always remain equal to or greater than V_{CC1} and V_{CC2}.

The FXLA2203 I/O pins must be driven by open-drain drivers on the host sides and the card sides.

SIM Slot Power Switch Truth Table

If EN=1 and **CH_Swap=1**; then the V_{CC} of SIM Slot 1 (VCC_Card_1) tracks the VCC1 voltage (ext. LDO), while the V_{CC} of SIM Slot 2 (VCC_Card_2) tracks the VCC2 voltage (ext. LDO). If EN=1 and **CH_Swap=0**; then the V_{CC} of SIM Slot 1 (VCC_Card_1) tracks the VCC2 voltage (ext. LDO), while the VCC of SIM Slot 2 (VCC_Card_2) tracks the VCC1 voltage (ext. LDO). *See Table 7.* Note that V_{CC} must be $\geq$ V_{CC1} and V_{CC2}.

SIM Slot Signal Truth Table

If EN=1 and CH_Swap=1, the Host 1 Input signal pins (CLK_H_1, RST_H_1, and I/O_H_1) are translated to the SIM Slot 1 output signal pins (CLK_1, RST_1, and I/O_1). The VCC1 voltage (ext. LDO) sets the voltage levels of CLK_1, RST_1, and I/O_1. Host 2 input signal pins (CLK_H_2, RST_H_2, and I/O_H_2) are translated to the SIM Slot 2 output signal pins (CLK_2, RST_2, and I/O_2). The VCC2 (ext. LDO) voltage sets the voltage levels of CLK_2, RST_2 and I/O_2.

If EN=1 and CH_Swap=0, the Host 1 input signal pins (CLK_H_1, RST_H_1 and I/O_H_1) is translated to the SIM Slot 2 output signal pins (CLK_2, RST_2, and I/O_2). The VCC1 voltage (ext. LDO) sets the voltage levels of CLK_2, RST_2, and I/O_2. Host 2 input signal pins (CLK_H_2, RST_H_2, and I/O_H_2) are translated to the SIM Slot 1 output signal pins (CLK_1, RST_1, and I/O_1). The VCC2 (ext. LDO) voltage sets the voltage levels of CLK_1, RST_1, and I/O_1.

Table 6. Power Switch Truth Table

VCC1	VCC2	EN	CH_Swap	VCC_Card 1	VCC_Card 2
0V – 3.6V	0V – 3.6V	1	1	VCC1	VCC2
0V – 3.6V	0V – 3.6V	1	0	VCC2	VCC1

Table 7. Signal Truth Table

EN	CH_Swap	SIM SLOT 1	SIM Slot 2
1	1	CLK_H_1, RST_H_1, and I/O_H_1	CLK_H_2, RST_H_2, and I/O_H_2
1	0	CLK_H_2, RST_H_2, and I/O_H_2	CLK_H_1, RST_H_1, and I/O_H_1

SIM Slot Signals: Active vs. 3-State

The individual SIM slot signals (CLK, RST, and I/O) are active only if the appropriate VCCn **and** VCC_H_n supplies are active (1.65V – 3.6V).

For example, if EN=1 and CH_Swap is 1, SIM Slot 1 signals (CLK_1, RST_1, and I/O_1) are active only if VCC1 and VCC_H_1 are both active (1.65V – 3.6V). VCC1 sets the voltage levels of CLK_1, RST_1, and I/O_1. If either VCC1 or VCC_H_1 is below 1.65V, SIM Slot 1 signals (CLK_1, RST_1, and I/O_1) are high impedance. Likewise, SIM Slot 2 signals (CLK_2, RST_2, and I/O_2) are active only if both VCC2 and VCC_H_2 are active (1.65V – 3.6V). VCC2 sets the voltage levels of CLK_2, RST_2, and I/O_2.

If EN=1 and CH_Swap is 0, SIM Slot 1 (CLK_1, RST_1, and I/O_1) signals are active only if VCC2 and VCC_H_2 are active (1.65V – 3.6V). VCC2 sets the voltage levels of CLK_1, RST_1, and I/O_1. Likewise, SIM Slot 2 signals (CLK_2, RST_2, and I/O_2) are active only if both VCC1 and VCC_H_1 are active (1.65V – 3.6V). VCC1 sets the voltage levels of CLK_2, RST_2, and I/O_2.

For a complete listing of all the possible power switch and signal combinations, see Table 8.

Table 8. Complete Power Switch and Signal Truth Table

Condition	Inputs							Outputs			
	VCC	EN	CH_SWAP	VCC_H_1	VCC_H_2	VCC1	VCC2	CLK_1, RST_1, I/O_1	CLK_2, RST_2, I/O_2	VCC_Card1	VCC_Card2
1	OFF	X	X	X	X	OFF	OFF	Z	Z	OFF	OFF
2	ON	L	X	X	X	X	X	Z	Z	Z	Z
3	ON	H	1	OFF	OFF	OFF	OFF	Z	Z	OFF	OFF
4	ON	H	1	OFF	OFF	ON	OFF	Z	Z	ON	OFF
5	ON	H	1	OFF	OFF	OFF	ON	Z	Z	OFF	ON
6	ON	H	1	OFF	OFF	ON	ON	Z	Z	ON	ON
7	ON	H	1	OFF	ON	OFF	OFF	Z	Z	OFF	OFF
8	ON	H	1	OFF	ON	ON	OFF	Z	Z	ON	OFF
9	ON	H	1	OFF	ON	OFF	ON	Z	A	OFF	ON
10	ON	H	1	OFF	ON	ON	ON	Z	A	ON	ON
11	ON	H	1	ON	OFF	OFF	OFF	Z	Z	OFF	OFF
12	ON	H	1	ON	OFF	ON	OFF	A	Z	ON	OFF
13	ON	H	1	ON	OFF	OFF	ON	Z	Z	OFF	ON
14	ON	H	1	ON	OFF	ON	ON	A	Z	ON	ON
15	ON	H	1	ON	ON	OFF	OFF	Z	Z	OFF	OFF
16	ON	H	1	ON	ON	ON	OFF	A	Z	ON	OFF
17	ON	H	1	ON	ON	OFF	ON	Z	A	OFF	ON
18	ON	H	1	ON	ON	ON	ON	A	A	ON	ON
19	ON	H	0	OFF	OFF	OFF	OFF	Z	Z	OFF	OFF
20	ON	H	0	OFF	OFF	ON	OFF	Z	Z	OFF	ON
21	ON	H	0	OFF	OFF	OFF	ON	Z	Z	ON	OFF
22	ON	H	0	OFF	OFF	ON	ON	Z	Z	ON	ON
23	ON	H	0	OFF	ON	OFF	OFF	Z	Z	OFF	OFF
24	ON	H	0	OFF	ON	ON	OFF	Z	Z	OFF	ON
25	ON	H	0	OFF	ON	OFF	ON	A	Z	ON	OFF
26	ON	H	0	OFF	ON	ON	ON	A	Z	ON	ON
27	ON	H	0	ON	OFF	OFF	OFF	Z	Z	OFF	OFF
28	ON	H	0	ON	OFF	ON	OFF	Z	A	OFF	ON
29	ON	H	0	ON	OFF	OFF	ON	Z	Z	ON	OFF
30	ON	H	0	ON	OFF	ON	ON	Z	A	ON	ON
31	ON	H	0	ON	ON	OFF	OFF	Z	Z	OFF	OFF
32	ON	H	0	ON	ON	ON	OFF	Z	A	OFF	ON
33	ON	H	0	ON	ON	OFF	ON	A	Z	ON	OFF
34	ON	H	0	ON	ON	ON	ON	A	A	ON	ON

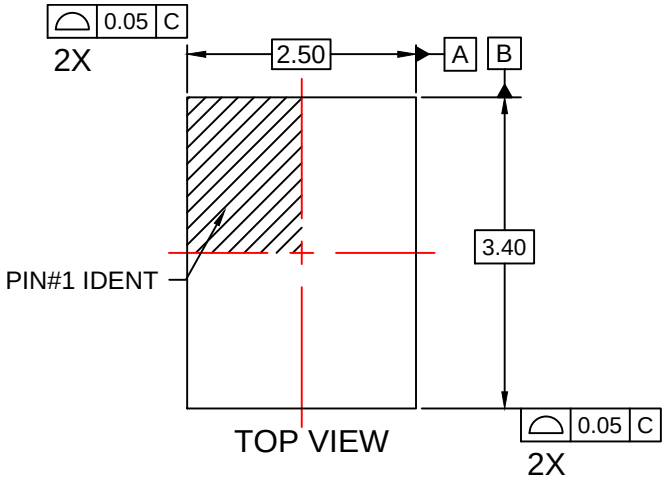
Notes:

29. ON=1.65V – 3.6V.
30. OFF=Powered down or 0V.
31. X=Don't Care.
32. $V_{CC} \geq V_{CC1}$ and V_{CC2}.

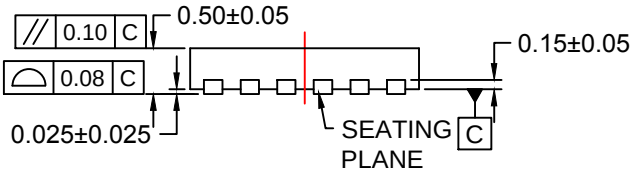
Product-Specific Dimensions

Product-Specific Dimensions

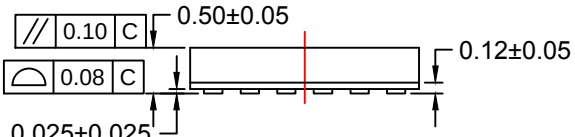
Description	Nominal Values (mm)	Description	Nominal Values (mm)
Overall Height	0.50	Lead Length	0.40
PKG Standoff	0.012	Lead Pitch	0.40
Lead Thickness	0.15	Body Length (X)	2.50
Lead Width	0.20	Body Width (Y)	3.40



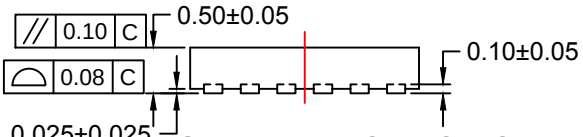
TOP VIEW



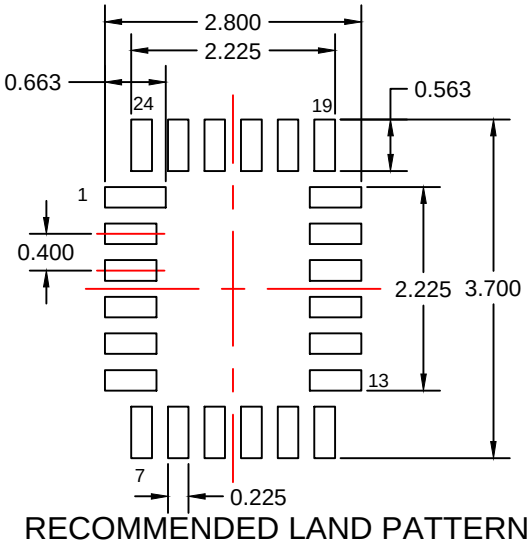
SIDE VIEW -OPTION A



SIDE VIEW -OPTION B



SIDE VIEW -OPTION C



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NOTES:

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B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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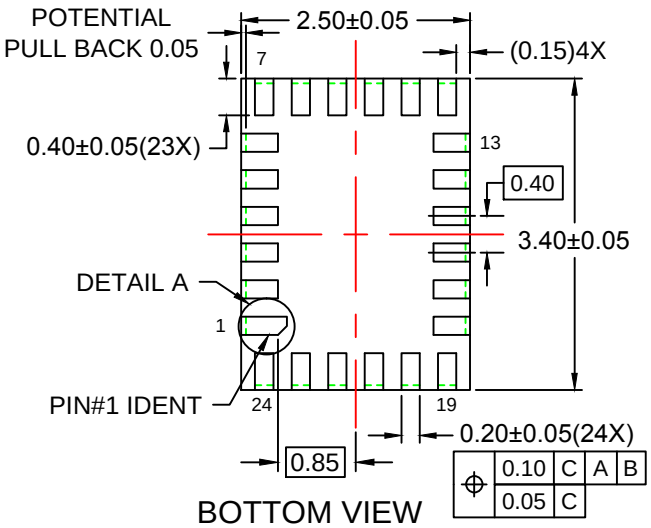
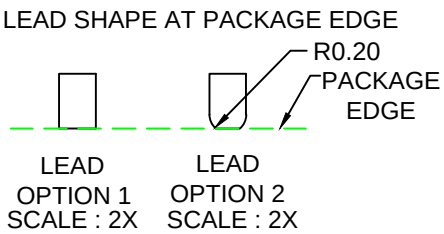
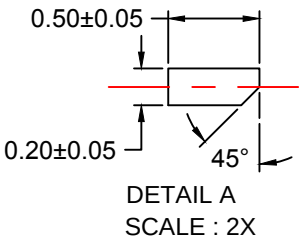


BOTTOM VIEW





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Definition of Terms

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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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