MOTOROLA

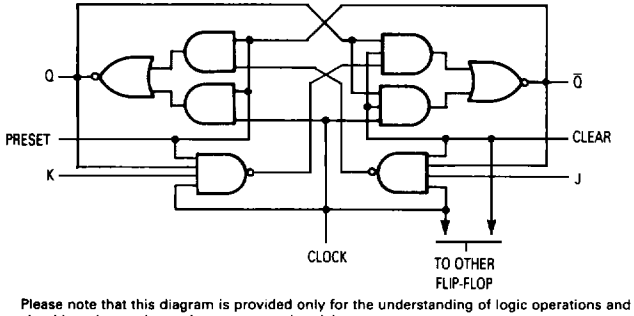
Military 54LS114A

Dual J-K Flip-Flop With Preset, Common Clear and Common Clock

MIL-M-38510/30105

The 54LS114A offers common clock and common clear inputs and individual J, K, and set inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM
(one half show)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

MODE SELECT — TRUTH TABLE

Operating Mode	Inputs				Outputs	
	$\overline{PR}$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

AVAILABLE AS:

1) JAN: JM38510/30105BXA
2) SMD: *
3) 883C: 54LS114A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2
***Call Factory for latest update**

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
CLR	1	1	2	GND
K_1	2	2	3	V_{CC}
J_1	3	3	4	V_{CC}
PR_1	4	4	6	GND
Q_1	5	5	8	V_{CC}
$\overline{Q}_1$	6	6	9	V_{CC}
GND	7	7	10	GND
$\overline{Q}_2$	8	8	12	V_{CC}
Q_2	9	9	13	V_{CC}
PR_2	10	10	14	GND
J_2	11	11	16	V_{CC}
K_2	12	12	18	V_{CC}
CLK	13	13	19	GND
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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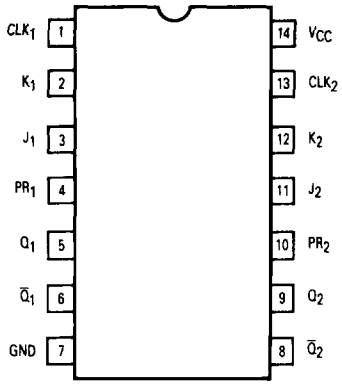
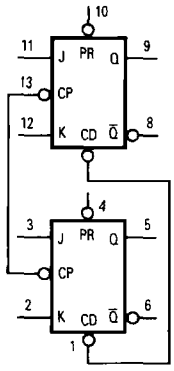
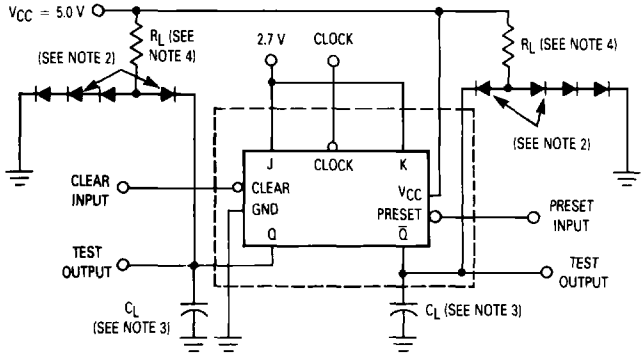
CONNECTION DIAGRAM



LOGIC SYMBOL

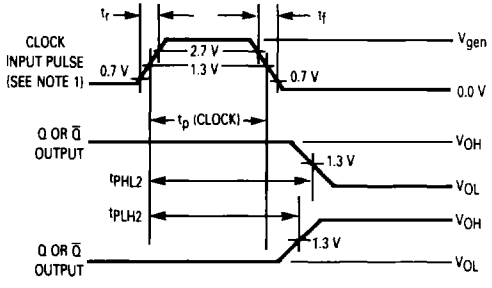


AC TEST CIRCUIT



Synchronous Switching Test Circuit

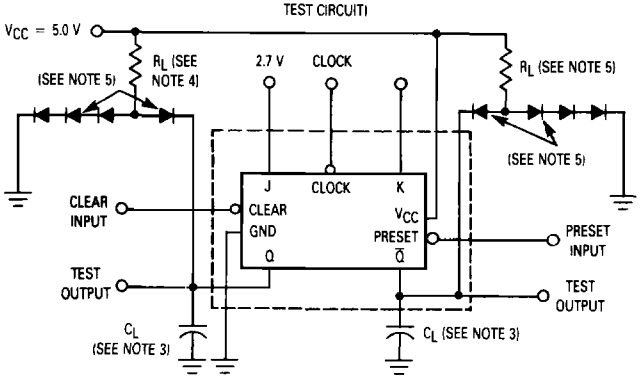
WAVEFORMS



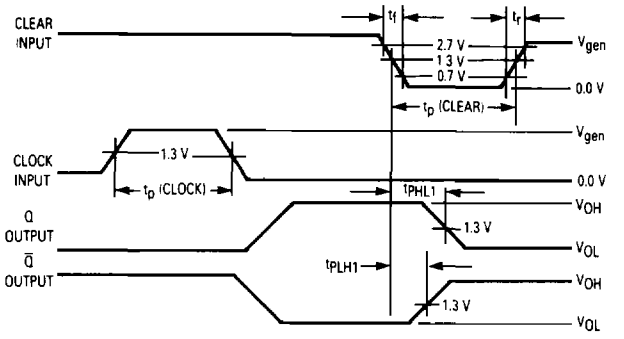
NOTES:
1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output): V_{gen} = 3.0 V, $t_r \leq$ 15 ns, t_f = 6.0 ns, t_p (clock) = 25 ns and PRR ≤ 1.0 MHz. When testing f_{MAX} the clock input characteristics are: V_{gen} = 3.0 V, $t_r = t_f \leq$ 6.0 ns, t_p (clock) ≤ 25 ns and PRR = (see table 1).
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 2.0 kΩ ± 5.0%.

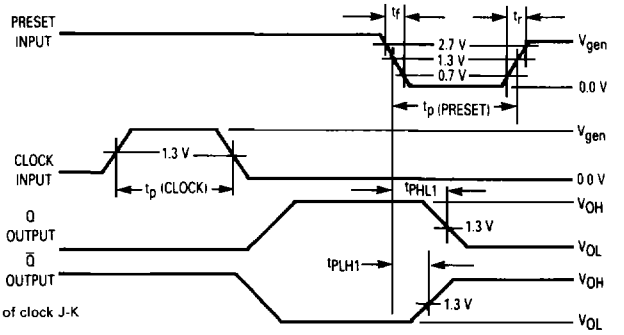
AC TEST CIRCUIT

(CLEAR & PRESET SWITCHING TEST CIRCUIT)



WAVEFORMS

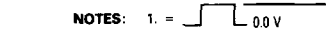


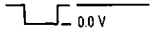


NOTES:

1. Clear or preset inputs dominate regardless of the state of clock J-K inputs.
2. Clear or preset input pulse characteristics: V_{gen} = 3.0 V, $t_f \leq 15$ ns, $t_r \leq 6.0$ ns, PRR ≤ 1.0 MHz, t_p (clear) = t_p (preset) = 30 ns, $Z_{out} \approx 50\ \Omega$.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 2.0 kΩ ± 5.0%.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset shall have a logical "1" voltage applied. When testing preset to output switching, clear input shall have a logical "1" voltage applied (see table 1).
7. Clock input pulse characteristics: t_p (clock) ≥ 25 ns, V_{gen} = 3.0 V, PRR ≤ 1.0 MHz.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −0.4 mA, V_{IN} = 2.0 V, V_{IL} = 0.7 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.7 V.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current (J & K inputs)		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other input = GND.
I_{IHH}	Logical "1" Input Current (J & K inputs)		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, (CLK, CLR & PR) = GND, other inputs are open.
I_{IH}	Logical "1" Input Current (PR inputs)		60		60		60	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, (CLK, J & K) = GND, other inputs are open.
I_{IHH}	Logical "1" Input Current (PR inputs)		300		300		300	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs = GND.
I_{IH}	Logical "1" Input Current (CLR inputs)		120		120		120	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = GND.
I_{IHH}	Logical "1" Input Current (CLR inputs)		600		600		600	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs = GND.
I_{IH}	Logical "1" Input Current (CLK inputs)		160		160		160	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = GND.
I_{IHH}	Logical "1" Input Current (CLK inputs)		800		800		800	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs = GND.
I_{IL}	Logical "0" Input Current (J & K inputs)	−0.12	−0.36	−0.12	−0.36	−0.12	−0.36	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, CLR = 4.5 V, J = GND, PR = (see note 2), other inputs are open.
I_{IL}	Logical "0" Input Current (PR inputs)	−0.12	−0.72	−0.12	−0.72	−0.12	−0.72	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, J & K = 4.5 V, CLK = 4.5 V, other inputs are open.
I_{IL}	Logical "0" Input Current (CLK inputs)	−0.24	−1.44	−0.24	−1.44	−0.24	−1.44	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs = 4.5 V, CLR = (see note 2).
I_{IL}	Logical "0" Input Current (CLR inputs)	−0.12	−1.5	−0.12	−1.5	−0.12	−1.5	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs = 4.5 V.
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, CLR = GND, V_{OUT} = 0 V, other inputs are open.
I_{CC}	Power Supply Current		8.0		8.0		8.0	mA	V_{CC} = 5.5 V, CLK = GND. V_{IN} = 5.5 V, (all inputs).
			8.0		8.0		8.0		V_{IN} = 5.5 V, PR = GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.

NOTES: 1. = 

2. = 

		Subgroup 7	Subgroup 8A	Subgroup 8B		
	Functional Tests					per Truth Table with V_{CC} = 4.5 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Output High-Low	5.0	28 20	5.0	40 35	5.0	40 35	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Output Low-High	5.0	21 20	5.0	32 27	5.0	32 27	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PHL2}	Propagation Delay /Data-Output Output High-Low	5.0	30	5.0	42	5.0	42	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH2}	Propagation Delay /Data-Output Output Low-High	5.0	22	5.0	32	5.0	32	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	25		25		25		MHz	V_{CC} = 5.0 V, V_{IN} = 2.7 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	30						MHz	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.

NOTES:
1. f_{MAX}, min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for C_L = 15 pF are guaranteed but not tested.