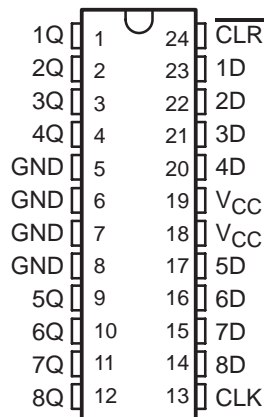


# 74ACT11273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

SCAS130 – D3443, MARCH 1990 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Flow-Through Architecture Optimizes PCB Layout
- Multiple Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE  
(TOP VIEW)



## description

These positive-edge-triggered flip-flops implement D-type flip-flop logic with a direct clear input.

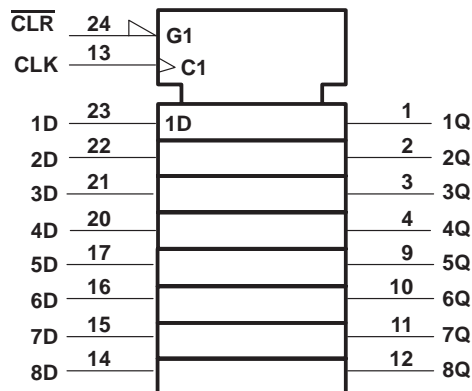
Data at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The 74ACT11273 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	$Q_0$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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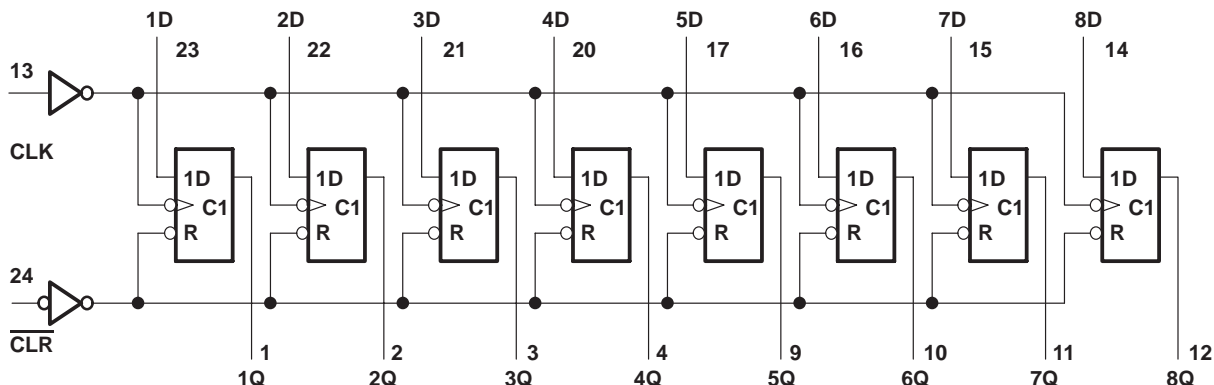
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# 74ACT11273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

SCAS130 – D3443, MARCH 1990 – REVISED APRIL 1993

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	- 0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	- 0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	- 0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 200$ mA
Storage temperature range .....	- 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## recommended operating conditions

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24	mA
$I_{OL}$	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	- 40	85	°C

**74ACT11273**  
**OCTAL D-TYPE FLIP-FLOP**  
**WITH CLEAR**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = - 50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I <sub>OH</sub> = - 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
I <sub>OH</sub> = - 75 mA <sup>†</sup>	5.5 V				3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V	0.1			0.1		V
		5.5 V	0.1			0.1		
	I <sub>OL</sub> = 24 mA	4.5 V	0.36			0.44		
		5.5 V	0.36			0.44		
	I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V				1.65		
I <sub>I</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	± 0.1			± 1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	8			80		μA
ΔI <sub>CC</sub> <sup>‡</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V	0.9			1		mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4					pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V<sub>CC</sub>.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f <sub>clock</sub>	Clock frequency	0	85	0	85	MHz
t <sub>w</sub>	Pulse duration	CLR low	5	5		ns
		CLK high or low	5.9	5.9		
t <sub>su</sub>	Setup time before CLK <sup>↑</sup>	Data high	4	4		ns
		Data low	5	5		
		CLR inactive	4	4		
t <sub>h</sub>	Hold time after CLK <sup>↑</sup>	1	1		ns	

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f <sub>max</sub>			85			85		MHz
t <sub>PHL</sub>	CLR	Any Q	4.4	9.5	12	4.4	13.3	ns
t <sub>PLH</sub>	CLK	Any Q	5.4	9.4	11.4	5.4	13.1	ns
t <sub>PHL</sub>			6	10.3	12.5	6	14.1	

**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

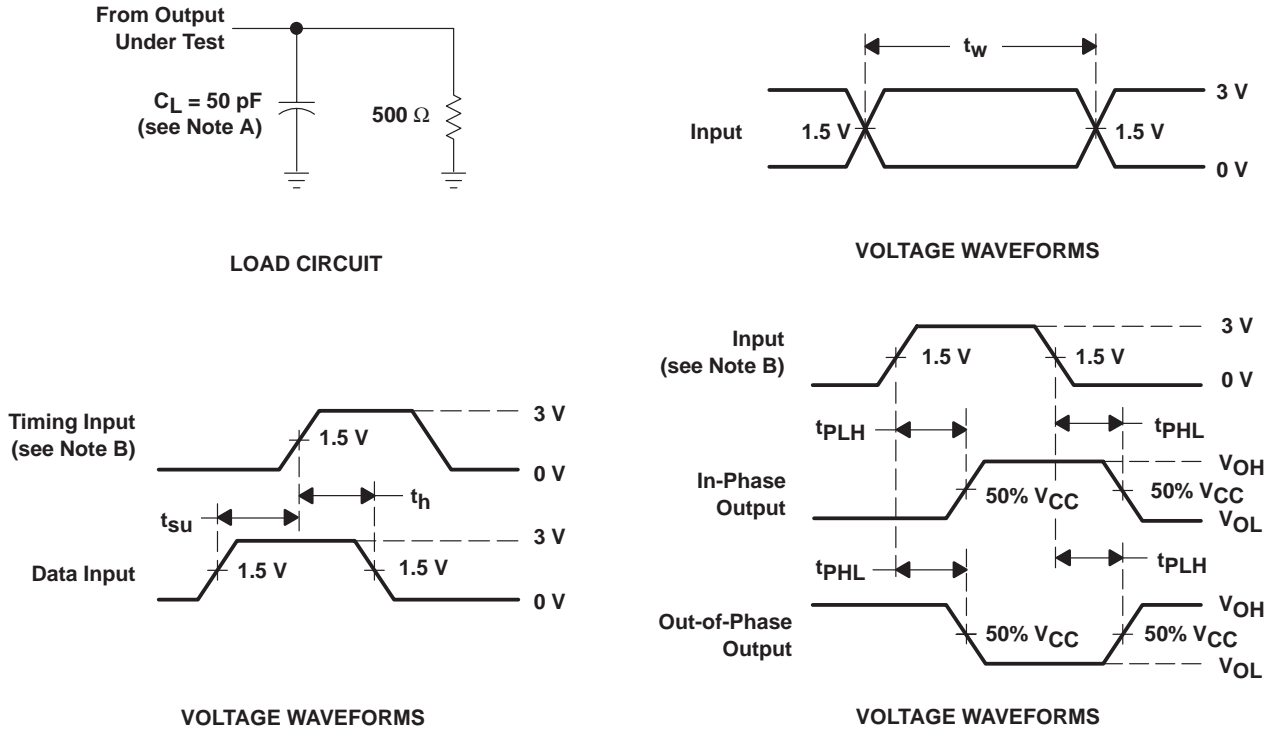
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	C <sub>L</sub> = 50 pF, f = 1 MHz	73	pF



**74ACT11273**  
**OCTAL D-TYPE FLIP-FLOP**  
**WITH CLEAR**

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**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ACT11273DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74ACT11273DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74ACT11273DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74ACT11273NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
74ACT11273NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

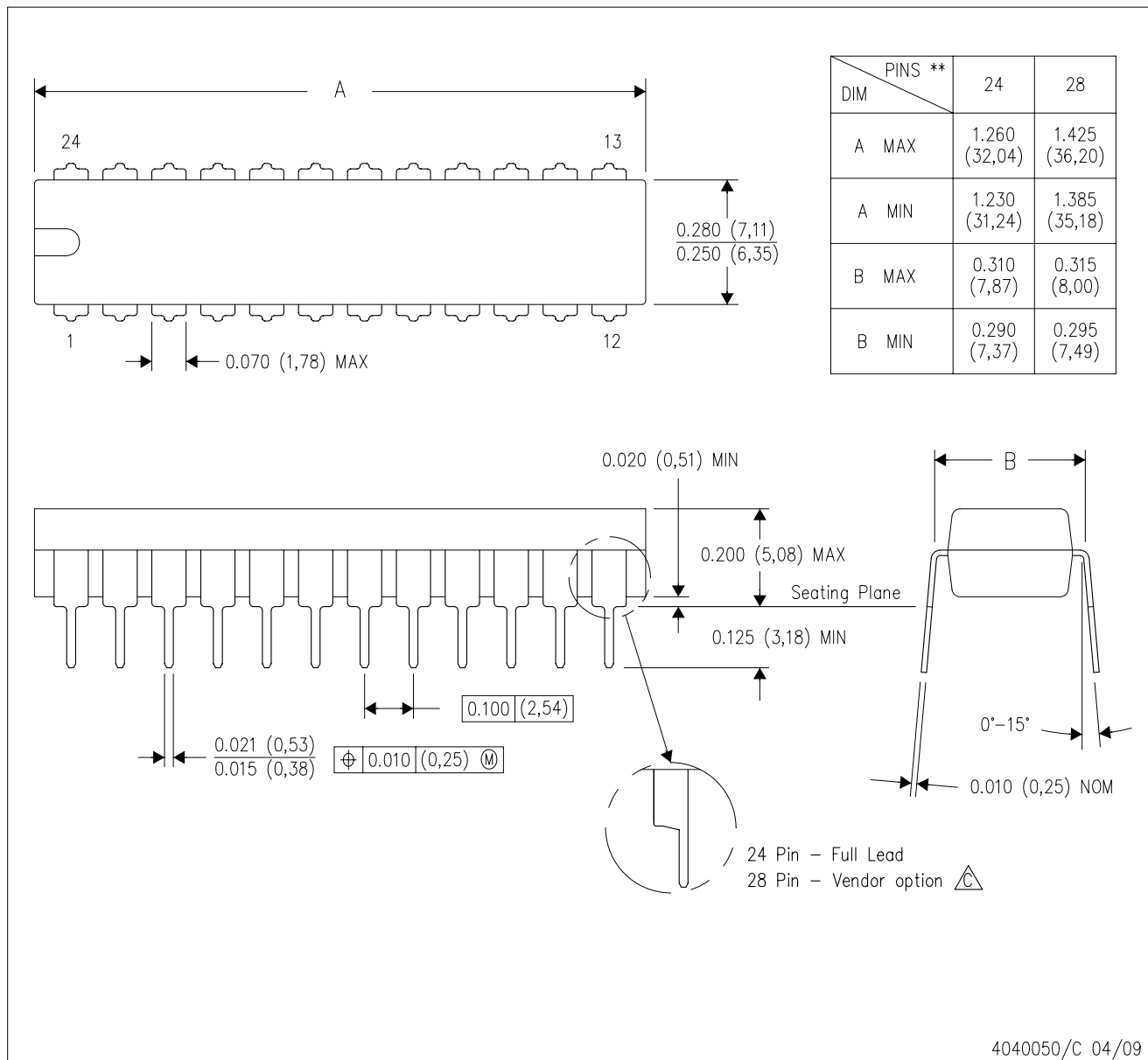
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# MECHANICAL DATA

NT (R-PDIP-T\*\*) 24 PINS SHOWN

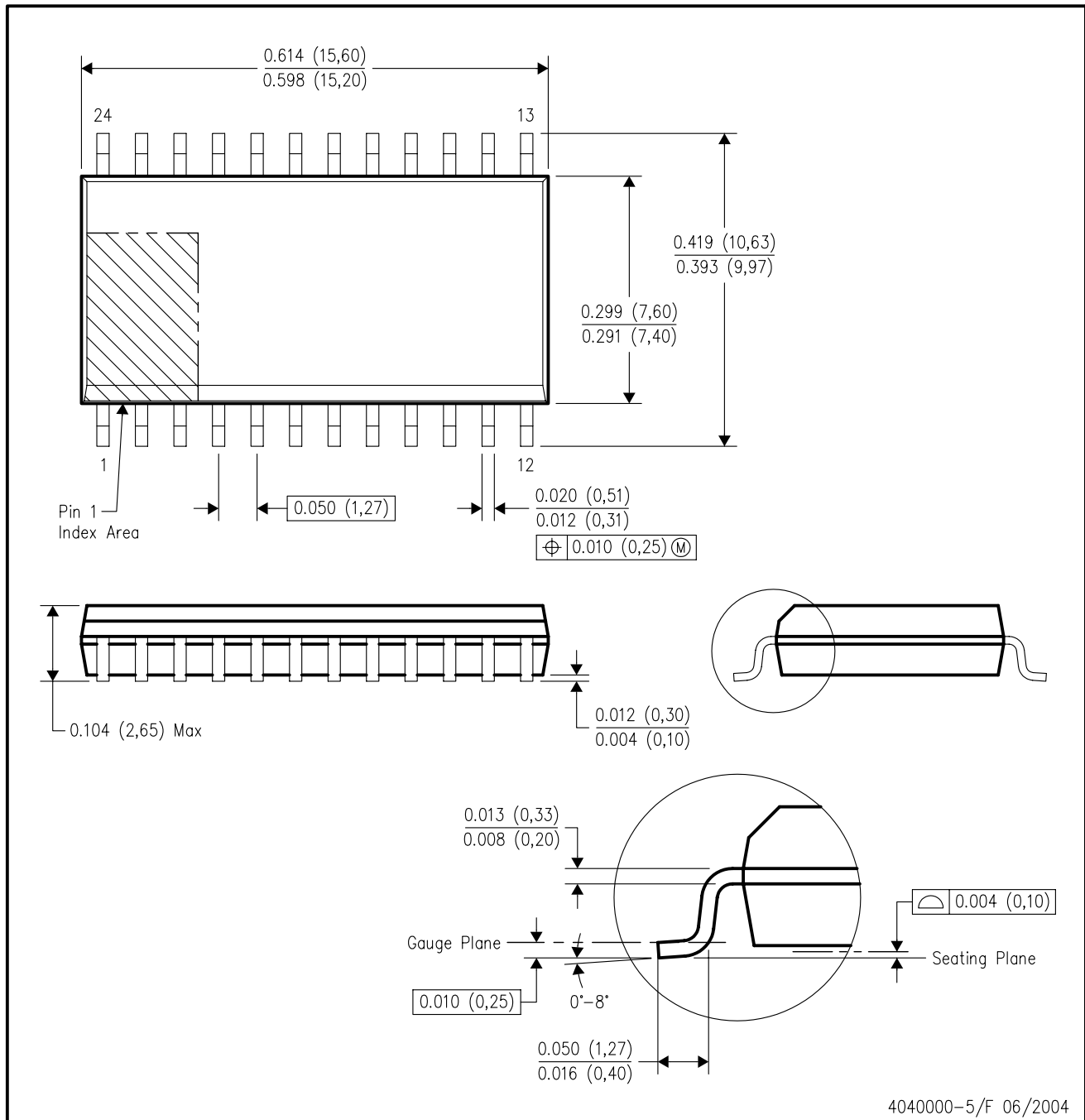
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - $\triangle$  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ACT11273DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74ACT11273DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74ACT11273DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74ACT11273NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
74ACT11273NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

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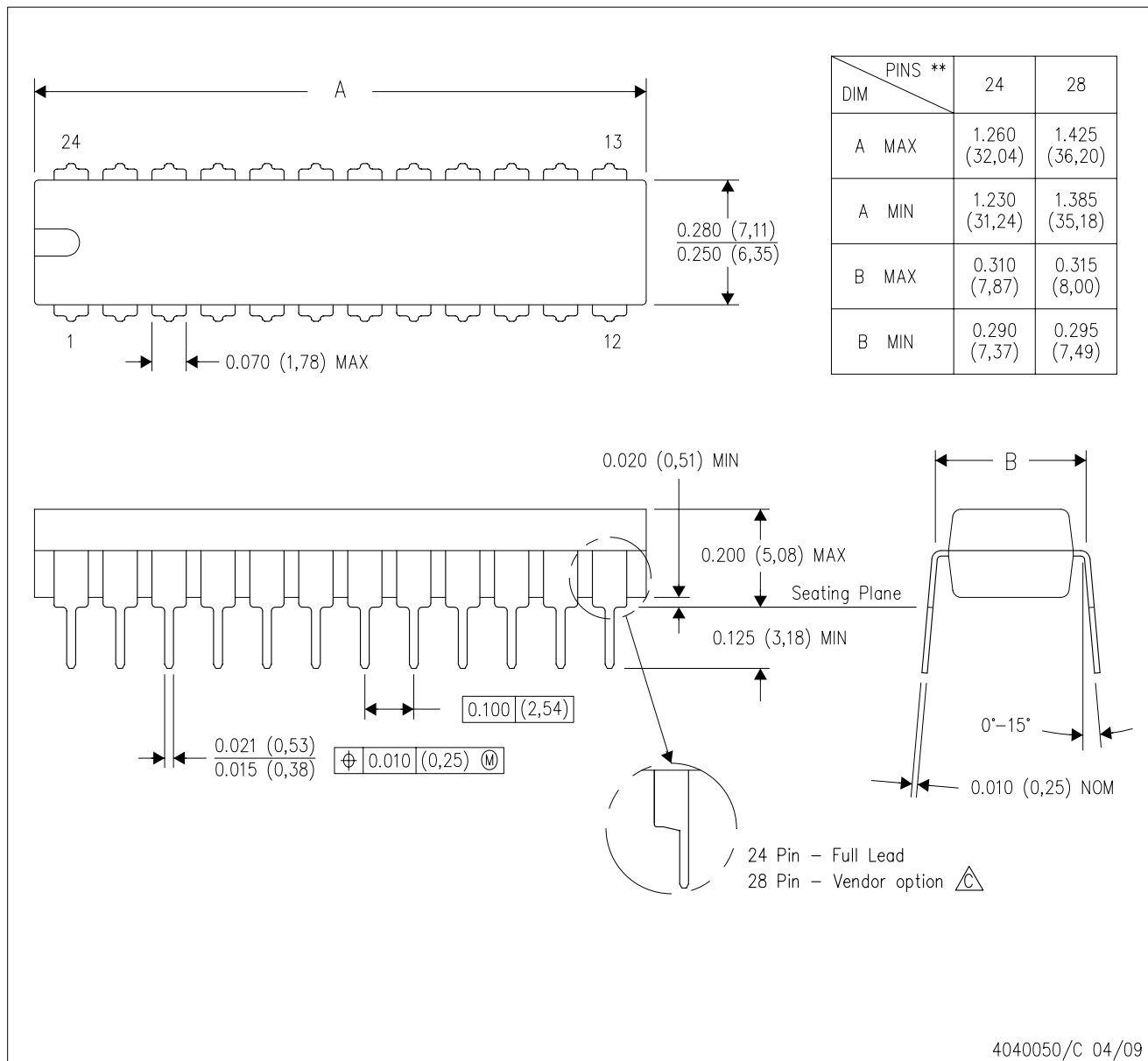


# MECHANICAL DATA


NT (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



4040050/C 04/09

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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