

MC74LV594A

8-Bit Shift Register with Output Register

The MC74LV594A is an 8-bit shift register designed for 2 V to 6.0 V V_{CC} operation. The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks (RCLK, SRCLK) and direct overriding clear (\overline{RCLR} , \overline{SRCLR}) inputs are provided on the shift and storage registers. A serial output (Q_H) is provided for cascading purposes.

The shift-register (SRCLK) and storage-register (RCLK) clocks are positive-edge triggered. If the clocks are tied together, the shift register always is one clock pulse ahead of the storage register.

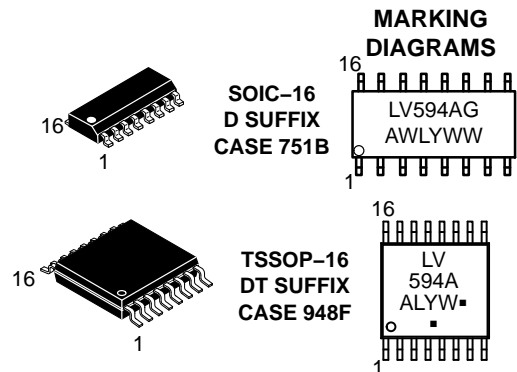
Features

- 2.0 V to 6.0 V V_{CC} Operation
- Low Input Current: 1.0 μ A
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C
- Support Mixed-Mode Voltage Operation on All Ports
- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Shift and Storage Registers
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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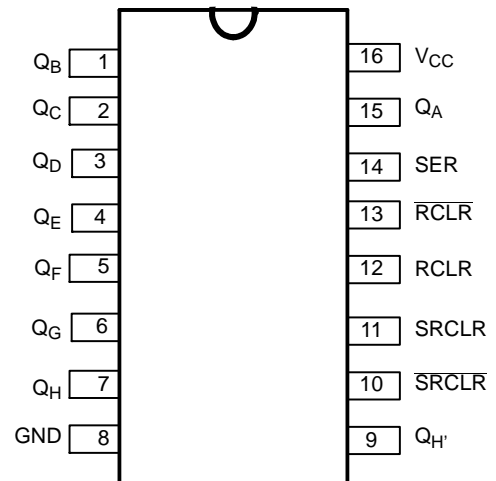
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A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

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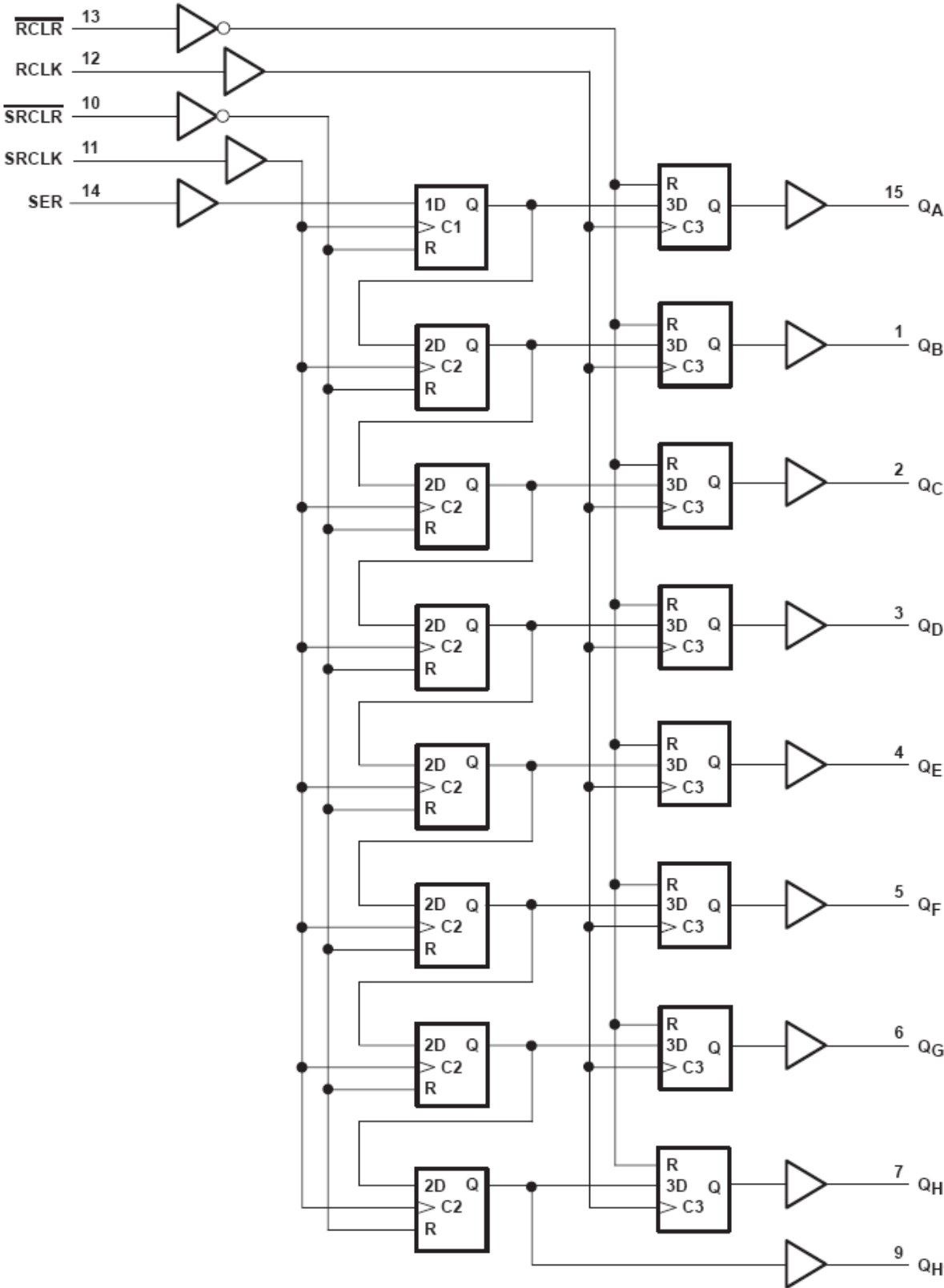


Figure 1. Logic Diagram

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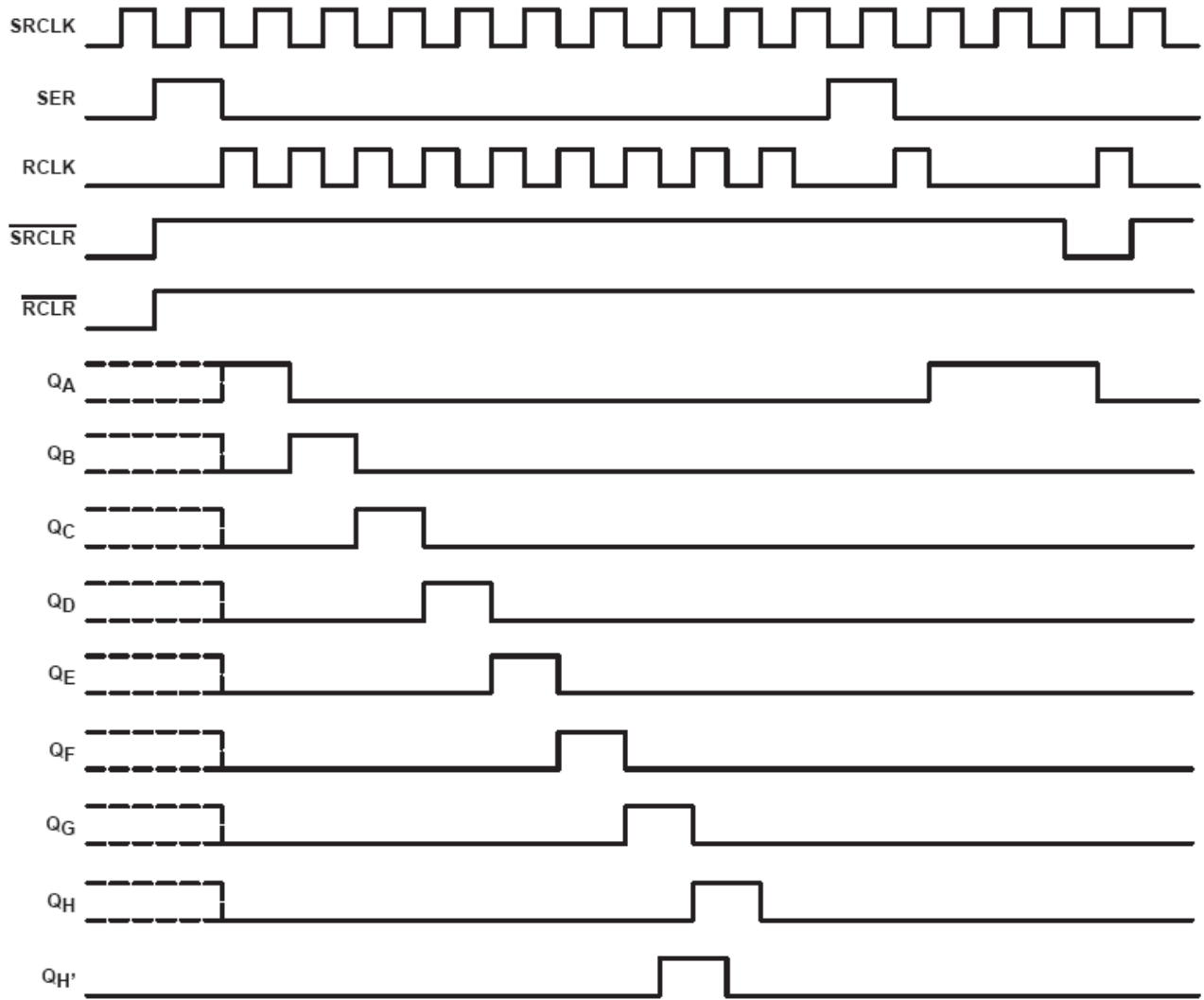


Figure 2. Timing Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC74LV594ADR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC74LV594ADTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage Active Mode (Note 1)	-0.5 to $V_{CC} + 0.5$	V
	High Impedance or Power-Off Mode	-0.5 to +7.0	
I_{IK}	DC Input Clamp Current	± 20	mA
I_{OK}	DC Output Clamp Current	± 35	mA
I_{IN}	DC Input Current	± 20	mA
I_O	DC Output Source / Sink Current	± 35	mA
I_{CC}	DC Supply Current per Supply Pin	± 75	mA
I_{GND}	DC Ground Current per Ground Pin	± 75	mA
T_{STG}	Storage Temperature Range	-65 to +150	$^{\circ}C$
T_L	Lead temperature, 1 mm from Case for 10 Seconds	260	$^{\circ}C$
T_J	Junction temperature under Bias	+150	$^{\circ}C$
θ_{JA}	Thermal Resistance SOIC TSSOP	112 148	$^{\circ}C$
P_D	Power Dissipation in Still Air at SOIC TSSOP	500 450	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 30% – 35%	UL-94-V0 (0.125 in)	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 3000 >400 N/A	V
$I_{Latchup}$	Latchup Performance Above V_{CC} and Below GND at 85 $^{\circ}C$ (Note 5)	± 300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS (Note 6)

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_I	DC Input Voltage (Referenced to GND)	0	V_{CC}	V
V_O	DC Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Free-Air Temperature	-55	+85	$^{\circ}C$
t_r, t_f	Input Rise or Fall Rate $V_{CC} = 2.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$	0 0 0	1000 500 400	nS

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} , (V)	Guaranteed Limits					Unit
				T _A = 25°C			T _A = -55°C to 125°C		
				Min	Typ	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0	1.5			1.5		V
			2.3 – 6.0	0.7 x V _{CC}			0.7 x V _{CC}		
V _{IL}	Maximum Low-Level Input Voltage		2.0			0.5		0.5	V
			2.3 – 6.0			0.3 x V _{CC}		0.3 x V _{CC}	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}							V
		I _{oH} = -50 μA	2.0 – 6.0	V _{CC} - 0.1			V _{CC} - 0.1		
		I _{oH} = -2 mA	2.3	2			2		
		I _{oH} = -6 mA	3.0	2.48			2.48		
		I _{oH} = -12 mA	4.5	3.8			3.8		
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}							V
		I _{oH} = 50 μA	2.0 – 6.0			0.1		0.1	
		I _{oH} = 2 mA	2.3			0.4		0.4	
		I _{oH} = 6 mA	3.0			0.44		0.44	
		I _{oH} = 12 mA	4.5			0.55		0.55	
I _{IN}	Maximum Input Leakage Current	V _I = V _{CC} or GND	6.0		±0.1		±1		μA
I _{CC}	Maximum Supply Current	V _I = V _{CC} or GND, I _O = 0 A	6.0			8.0		80	μA
C _I	Input Capacitance	V _I = V _{CC} or GND	3.3		3.5				pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TIMING SPECIFICATIONS (See Figure 3)

Symbol	Parameter	Conditions	V _{CC} , (V)	T _A = 25°C		T _A = -55°C to 125°C		Unit			
				Min	Max	Min	Max				
t _w	Pulse Duration	RCLK or SRCLK High or Low	2.3 – 2.7	7		7.5		ns			
			3.0 – 3.6	5.5		5.5					
			4.5 – 5.5	5		5					
		RCLR or SRCLR Low	2.3 – 2.7	6		6.5					
			3.0 – 3.6	5		5					
			4.5 – 5.5	5.2		5.2					
t _{su}	Setup Time	SER before SRCLK↑	2.3 – 2.7	5.5		5.5		ns			
			3.0 – 3.6	3.5		3.5					
			4.5 – 5.5	3		3					
		SRCLK↑ before RCLK↑	2.3 – 2.7	8		9					
			3.0 – 3.6	8		8.5					
			4.5 – 5.5	5		5					
		SRCLR Low before RCLK↑	2.3 – 2.7	8.5		9.5					
			3.0 – 3.6	8		9					
			4.5 – 5.5	5		5					
		SRCLR High (Inactive) before SRCLK↑	2.3 – 2.7	6		6.8					
			3.0 – 3.6	4.2		4.8					
			4.5 – 5.5	2.9		3.3					
		RCLR High (Inactive) before RCLK↑	2.3 – 2.7	6.7		7.6					
			3.0 – 3.6	4.6		5.3					
			4.5 – 5.5	3.2		3.7					
		t _H	Hold Time	SER after SRCLK↑	2.3 – 2.7	1.5			1.5		ns
					3.0 – 3.6	1.5			1.5		
					4.5 – 5.5	2			2		

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AC CHARACTERISTICS (See Figure 3)

Symbol	Parameter	Load Conditions	Input to Output	V _{CC} (V)	Guaranteed Limits					Unit
					T _A = 25°C			T _A = -55°C to 125°C		
					Min	Typ	Max	Min	Max	
f _{MAX}		C _L = 15 pF		2.3 – 2.7	65	80		45		MHz
				3.0 – 3.6	80	120		70		
				4.5 – 5.5	135	170		115		
		C _L = 50 pF		2.3 – 2.7	50	51		40		
				3.0 – 3.6	70	74		55		
				4.5 – 5.5	115	120		90		
t _{PLH}	Propagation Delay Low to High	C _L = 15 pF	RCLK to Q _A -Q _H	2.3 – 2.7			27.5	1	32.5	ns
				3.0 – 3.6			18	1	22.5	
				4.5 – 5.5			12	1	15	
			SRCLK to Q _H '	2.3 – 2.7			27.5	1	32	
				3.0 – 3.6			18	1	22	
				4.5 – 5.5			12.5	1	12	
		C _L = 50 pF	RCLK to Q _A -Q _H	2.3 – 2.7		22.1	25.0	1	30.0	
				3.0 – 3.6		15.6	17.5	1	21.0	
				4.5 – 5.5		11.5	12.5	1	15.5	
			SRCLK to Q _H '	2.3 – 2.7		21.6	25.5	1	29.5	
				3.0 – 3.6		15.2	18.0	1	21.0	
				4.5 – 5.5		10.9	12.5	1	15.0	
t _{PHL}	Propagation Delay High to Low	C _L = 15 pF	RCLK to Q _A -Q _H	2.3 – 2.7			23	1	27.5	ns
				3.0 – 3.6			15.5	1	19	
				4.5 – 5.5			11	1	14	
			SRCLK to Q _H '	2.3 – 2.7			23.5	1	27	
				3.0 – 3.6			16	1	19	
				4.5 – 5.5			11	1	13.5	
			RCLR to Q _A -Q _H	2.3 – 2.7			20.5	1	25	
				3.0 – 3.6			14.5	1	17.5	
				4.5 – 5.5			10	1	12	
			SRCLR to Q _H '	2.3 – 2.7				1	23	
				3.0 – 3.6			13	1	16	
				4.5 – 5.5			9	1	11	
		C _L = 50 pF	RCLK to Q _A -Q _H	2.3 – 2.7		19.7	23.0	1	27.0	
				3.0 – 3.6		14.0	16.5	1	19.5	
				4.5 – 5.5		10.1	11.5	1	13.5	
			SRCLK to Q _H '	2.3 – 2.7		18.4	21.5	1	25.0	
				3.0 – 3.6		13.1	15.0	1	18.0	
				4.5 – 5.5		9.0	10.5	1	12.5	
			RCLR to Q _A -Q _H	2.3 – 2.7		25.7	30.0	1	35.0	
				3.0 – 3.6		17.6	20.0	1	24.5	
				4.5 – 5.5		12.2	13.5	1	17.0	
			SRCLR to Q _H '	2.3 – 2.7		25.3	30.0	1	34	
				3.0 – 3.6		17.3	20.0	1	24.0	
				4.5 – 5.5		11.9	14.0	1	16.5	

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NOISE CHARACTERISTICS, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

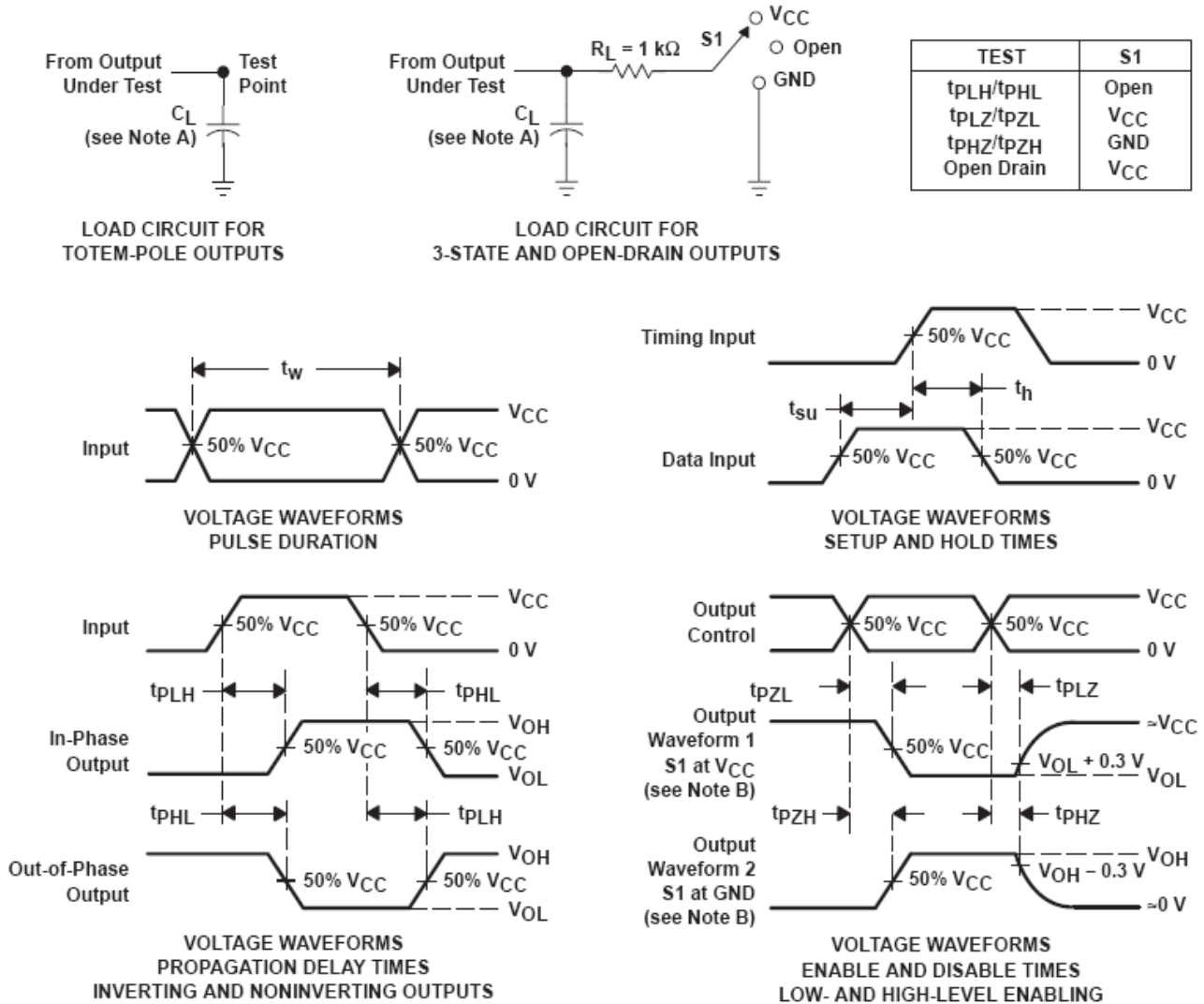
Symbol	Parameter	Min	Typ	Max	Unit
$V_{OL(P)}$	Quiet Output, Maximum Dynamic V_{OL}		0.8	0.8	V
$V_{OL(V)}$	Quiet Output, Minimum Dynamic V_{OL}		-0.1	-0.8	V
$V_{OH(V)}$	Quiet Output, Minimum Dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-Level Dynamic Input Voltage	2.31			V
$V_{IL(D)}$	Low-Level Dynamic Input Voltage			0.99	V

POWER DISSIPATION CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	V_{CC} (V)	Typ	Unit
C_{PD}	Power Dissipation Capacitance	f = 10 MHz	3.3	93	pF
			5	112	

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PARAMETER MEASUREMENT INFORMATION

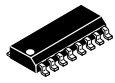


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

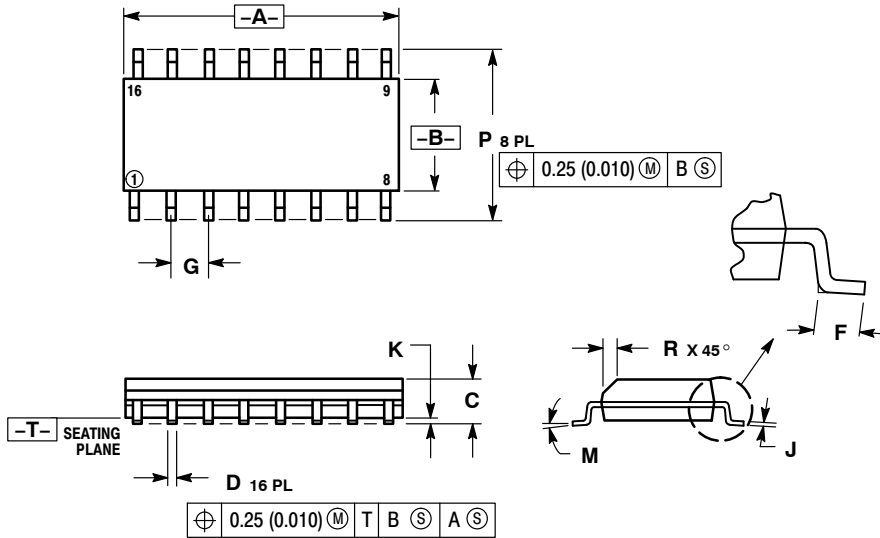
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SCALE 1:1

SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



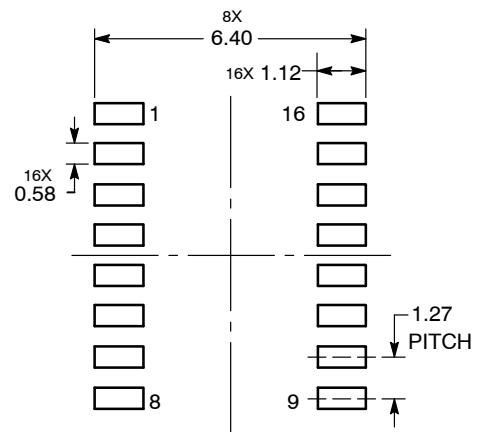
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- | | | | |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p> | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p> | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> | |

SOLDERING FOOTPRINT

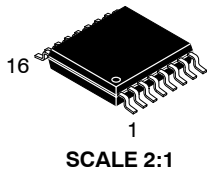


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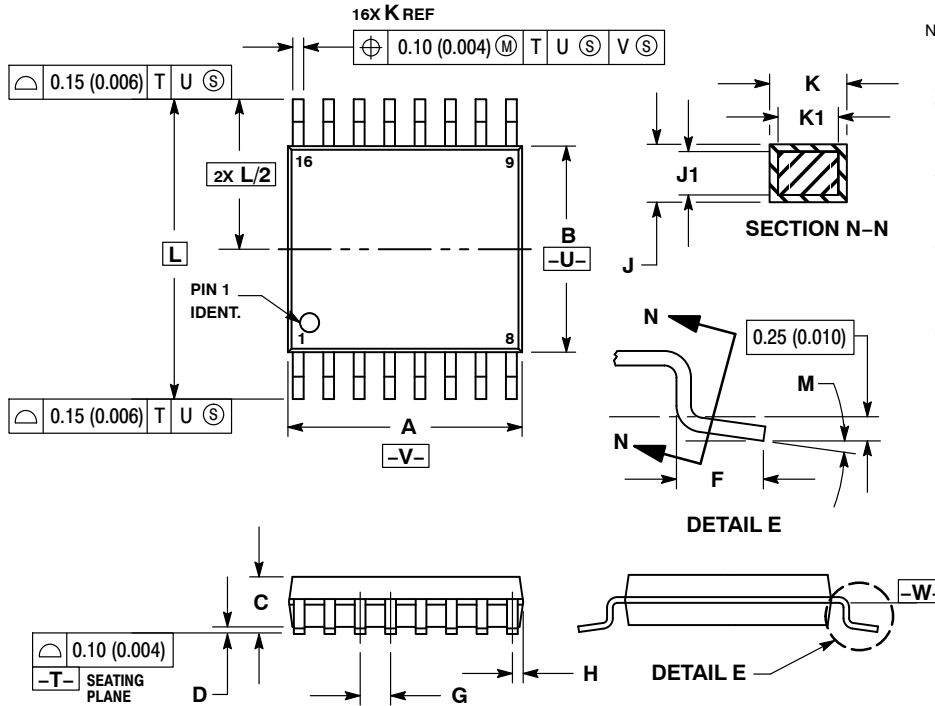
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16
CASE 948F-01
ISSUE B

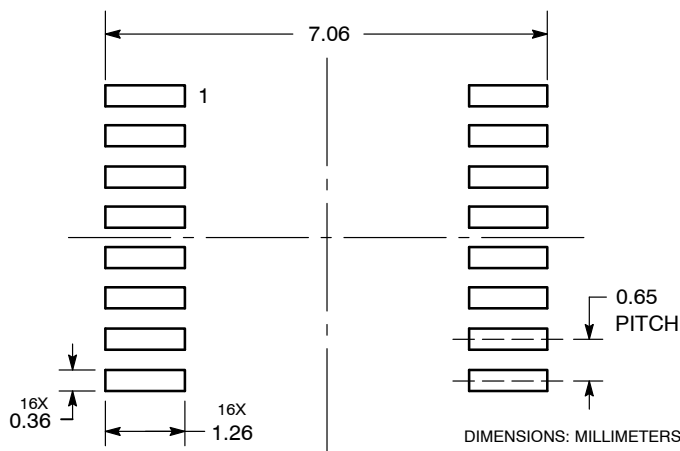
DATE 19 OCT 2006



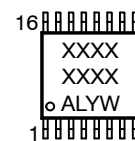
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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