011192

54LS/74LS502

8-BIT SUCCESSIVE APPROXIMATION REGISTER

DESCRIPTION — The 'LS502 is an 8-bit register with the interstage logic necessary to perform serial-to-parallel conversion and provide an active LOW Conversion Complete ($\overline{CC}$) signal coincident with storage of the eighth bit. An active LOW Start ($\overline{S}$) input performs synchronous initialization which forces Q_7 LOW and all other outputs HIGH. Subsequent clocks shift this Q_7 LOW signal downstream which simultaneously backfills the register such that the first serial data (D input) bit is stored in Q_7, the second bit in Q_6, the third in Q_5, etc. The serial input data is also synchronized by an auxiliary flip-flop and brought out on Q_D.

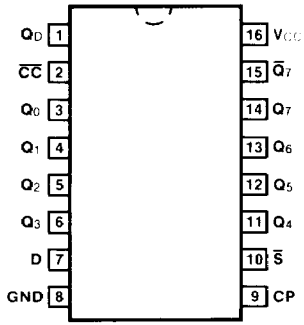
Designed primarily for use in the successive approximation technique for analog-to-digital conversion, the 'LS502 can also be used as a serial-to-parallel converter ring counter and as the storage and control element in recursive digital routines.

- **LOW POWER SCHOTTKY VERSION OF 2502**
- **STORAGE AND CONTROL FOR SUCCESSIVE APPROXIMATION A TO D CONVERSION**
- **PERFORMS SERIAL-TO-PARALLEL CONVERSION**

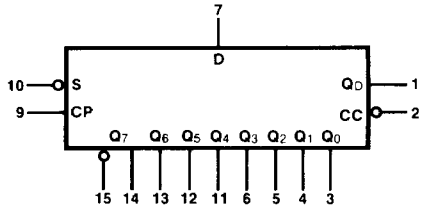
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS502PC		9B
Ceramic DIP (D)	A	74LS502DC	54LS502DM	6B
Flatpak (F)	A	74LS502FC	54LS502FM	4L

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL

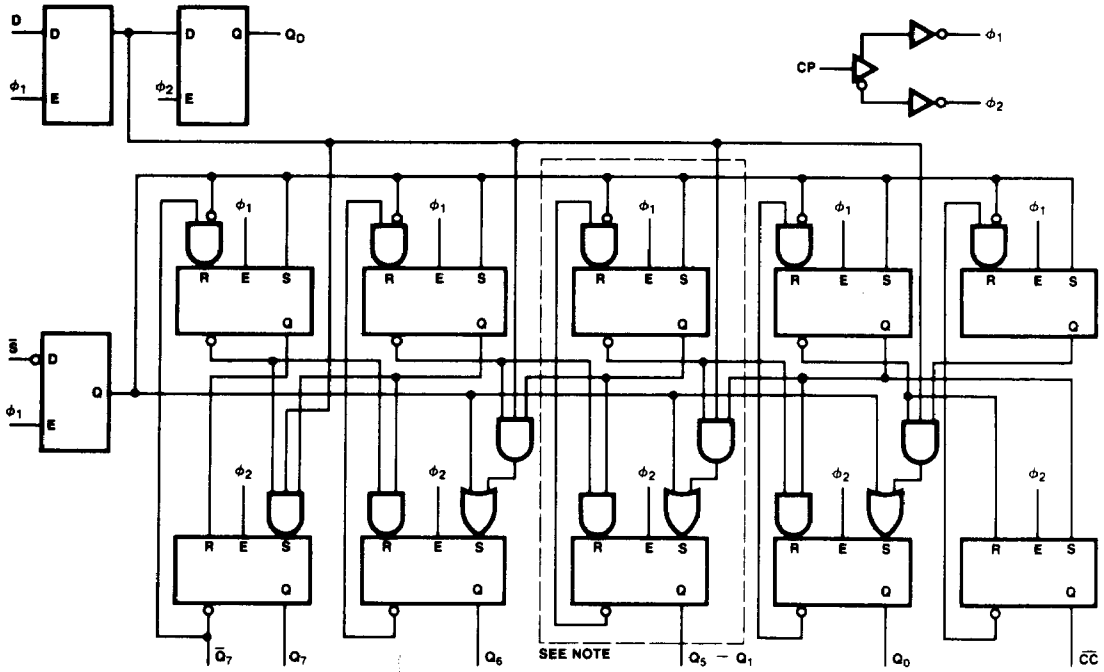


V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D	Serial Data Input	0.5/0.25
$\overline{S}$	Start Input (Active LOW)	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
Q_D	Synchronized Serial Data Output	10/5.0 (2.5)
$\overline{CC}$	Conversion Complete Output (Active LOW)	10/5.0 (2.5)
$Q_0 - Q_7$	Parallel Register Outputs	10/5.0 (2.5)
$\overline{Q}_7$	Complement of Q_7 Output	10/5.0 (2.5)

LOGIC DIAGRAM



Note: Cell logic is repeated for register stages Q_5 to Q_1.

FUNCTIONAL DESCRIPTION — The register stages are composed of transparent RS latches arranged in master/slave pairs. The master and slave latches are enabled separately by non-overlapping complementary signals ϕ_1 and ϕ_2 derived internally from the CP input. Master latches are enabled when CP is LOW and slave latches are enabled when CP is HIGH. Information is transferred from master to slave, and thus to the outputs, by the LOW-to-HIGH transition of CP.

Initializing the register requires a LOW signal on $\overline{S}$ while exercising CP. With $\overline{S}$ and CP LOW, all master latches are SET (Q side HIGH). A LOW-to-HIGH CP transition, with $\overline{S}$ remaining LOW, then forces the slave latches to the condition wherein Q_7 is LOW and all other register outputs, including $\overline{CC}$, are HIGH. This condition will prevail as long as $\overline{S}$ remains LOW, regardless of subsequent CP rising edge. To start the conversion process, $\overline{S}$ must return to the HIGH state. On the next CP rising edge, the information stored in the serial data input latch is transferred to Q_D and Q_7, while Q_6 is forced to the LOW state. On the rising edge of the next seven clocks, this LOW signal is shifted downstream, one bit at a time, while the serial data enters the register position one bit behind this LOW signal, as shown in the Truth Table. Note that after a serial data bit appears at a particular output, that register position undergoes no further changes. After the shifted LOW signal reaches $\overline{CC}$, the register is locked up and no further changes can occur until the register is initialized for the next conversion process.

Figure a shows a simplified hook-up of a 'LS502, a D/A converter and a comparator arranged to convert an analog input voltage into an 8-bit binary number by the successive approximation technique. *Figure b* is an idealized graph showing the various values that the D/A converter output voltage can assume in the course of the conversion. The vertical axis is calibrated in fractions of the full-scale output capability of the D/A converter and the horizontal axis represents the successive states of the Truth Table. At time t_1, Q_7 is LOW and $Q_6 - Q_0$ are HIGH, causing the D/A output to be one-half of full scale. If the analog input voltage is greater than this voltage the comparator output (hence the D input of the 'LS502) will be LOW, and at times t_2 the D/A output will rise to three-fourths of full scale because Q_7 will remain LOW and contribute 50% while Q_6 is forced LOW and contributes another 25%. On the other hand, if the analog input voltage is less than one-half of full scale, the comparator output will be HIGH and Q_7 will go HIGH at t_2. Q_6 will still be forced LOW at t_2, and the D/A output will decrease to 25% of full scale. Thus with each successive clock, the D/A output will change by smaller increments. When the conversion is completed at t_9, the binary number represented by the register outputs will be the numerator of the fraction n/256, representing the analog input voltage as a fraction of the fullscale output D/A converter.

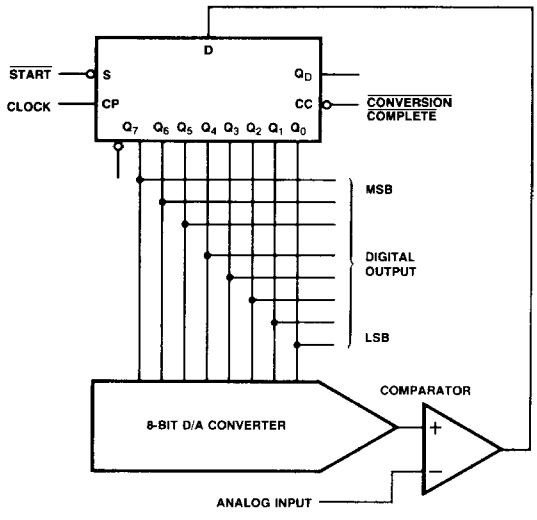


Fig. a

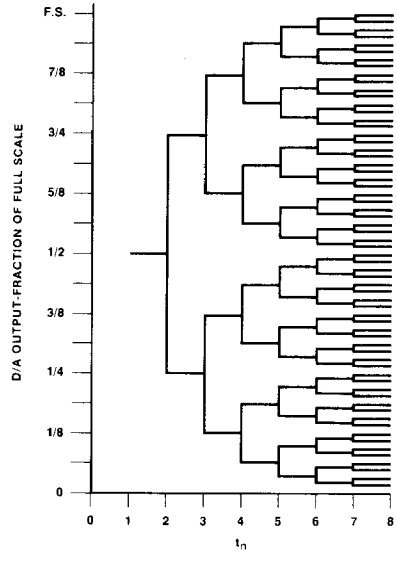


Fig. b

TRUTH TABLE

Time	INPUTS		OUTPUTS									
t_n	D	$\overline{S}$	Q_D	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	X	L	H	H	H	H	H	H	H	H
2	D_6	H	D_7	D_7	L	H	H	H	H	H	H	H
3	D_6	H	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	H	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

4

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		65	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for U.L. waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	15		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n or $\overline{CC}$		38 28	ns	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{S}$ to CP	16 16		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{S}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D to CP	8.0 8.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D to CP	10 10		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 46		ns	Fig. 3-8