## 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The MC74F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The F194 is similar in operation to the S195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

- Typical Shift Frequency of 150 MHz
- Asynchronous Master Reset
- Hold (Do Nothing) Mode
- Fully Synchronous Serial or Parallel Data Transfers


## FUNCTIONAL DESCRIPTION

The F194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select ( $\mathrm{S}_{0}, \mathrm{~S}_{1}$ ) inputs determine the type of operation, as shown in the Function Table. Signals on the Select, Parallel data $\left(\mathrm{P}_{0}-\mathrm{P}_{3}\right)$ and Serial data ( $\mathrm{D}_{\mathrm{SR}}$, $\mathrm{D}_{\mathrm{SL}}$ ) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset (MR) overrides all other inputs and forces the outputs LOW.


## FUNCTION TABLE

| Operating Mode | Inputs |  |  |  |  |  | Outputs |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MR | $\mathrm{S}_{1}$ | $\mathrm{S}_{0}$ | DSR | DSL | $\mathrm{P}_{\mathrm{n}}$ | $Q_{0}$ | $Q_{1}$ | $Q_{2}$ | Q ${ }^{\text {a }}$ |
| Reset | L | X | X | X | X | X | L | L | L | L |
| Hold | H | 1 | 1 | X | X | X | 90 | $\mathrm{q}_{1}$ | q2 | 93 |
| Shift Left | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & \mathrm{h} \\ & \mathrm{~h} \end{aligned}$ | I | $\begin{aligned} & \mathrm{X} \\ & \mathrm{x} \end{aligned}$ | h | $\begin{aligned} & \mathrm{X} \\ & \mathrm{x} \end{aligned}$ | $\begin{aligned} & \mathrm{q}_{1} \\ & \mathrm{q}_{1} \end{aligned}$ | $\begin{aligned} & \mathrm{q}_{2} \\ & \mathrm{q}_{2} \end{aligned}$ | $\begin{aligned} & \text { q3 } \\ & \text { q3 } \end{aligned}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ |
| Shift Right | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \end{aligned}$ | $1$ | $\begin{aligned} & \mathrm{h} \\ & \mathrm{~h} \end{aligned}$ | h | $\begin{aligned} & \mathrm{X} \\ & \mathrm{x} \end{aligned}$ | $\begin{aligned} & \mathrm{X} \\ & \mathrm{x} \end{aligned}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & \text { 90 } \\ & \text { q0 } \end{aligned}$ | $\begin{aligned} & \mathrm{q}_{1} \\ & \mathrm{q}_{1} \end{aligned}$ | $\begin{aligned} & \mathrm{q} 2 \\ & \mathrm{q} 2 \end{aligned}$ |
| Parallel Load | H | h | h | X | X | $\mathrm{p}_{\mathrm{n}}$ | $\mathrm{p}_{0}$ | p1 | P2 | P3 |

$I=$ LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
$h=$ HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
$p_{n}, q_{n}=$ Lower case letters indicate the state of the referenced input or output one setup
time prior to the LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
$X=$ Immaterial

## 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

FAST ${ }^{\text {T }}$ SCHOTTKY TTL


J SUFFIX
CERAMIC CASE 620-09


N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

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MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC
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LOGIC SYMBOL

$V_{C C}=$ PIN 16
$\mathrm{GND}=\mathrm{PIN} 8$

LOGIC DIAGRAM


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## GUARANTEED OPERATING RANGES

| Symbol | Parameter |  | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 74 | 4.5 | 5.0 | 5.5 | V |
| $\mathrm{~T}_{\mathrm{A}}$ | Operating Ambient Temperature Range | 74 | 0 | 25 | 70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\mathrm{OH}}$ | Output Current - High | 74 |  |  | -1.0 | mA |
| $\mathrm{I}_{\mathrm{OL}}$ | Output Current - Low | 74 |  |  | 20 | mA |

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | Limits |  |  | Unit | Test Conditions |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |  |
| $\mathrm{V}_{\text {IH }}$ | Input HIGH Voltage | 2.0 |  |  | V | Guaranteed Input | HIGH Voltage |
| $\mathrm{V}_{\text {IL }}$ | Input LOW Voltage |  |  | 0.8 | V | Guaranteed Inp | LOW Voltage |
| $\mathrm{V}_{\text {IK }}$ | Input Clamp Diode Voltage |  |  | -1.2 | V | $\mathrm{I} \mathrm{N}=-18 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | Output HIGH Voltage | 2.5 | 3.4 |  | V | $\mathrm{IOH}=-1.0 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$ |
|  |  | 2.7 | 3.4 |  | V | $\mathrm{I} \mathrm{OH}=-1.0 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{~V}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Output LOW Voltage |  | 0.35 | 0.5 | V | $\mathrm{IOL}=20 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ |
| ${ }_{\text {IH }}$ | Input HIGH Current |  |  | 20 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {IN }}=2.7 \mathrm{~V}$ | $V_{C C}=$ MAX |
|  |  |  |  | 100 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {IN }}=7.0 \mathrm{~V}$ |  |
| IIL | Input LOW Current |  |  | -0.6 | mA | $\mathrm{V}_{\text {IN }}=0.5 \mathrm{~V}$ | $V_{C C}=$ MAX |
| Ios | Output Short Circuit Current (Note 2) | -60 |  | -150 | mA | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{CC}}=$ MAX |
| ICC | Power Supply Current |  | 33 | 46 | mA | $\begin{aligned} & \hline \mathrm{S}_{\mathrm{n}}, \mathrm{MR}, \mathrm{DSR}^{2}, \\ & \mathrm{DSL}=4.5 \mathrm{~V} \\ & \mathrm{P}_{\mathrm{n}}=\mathrm{Gnd}, \\ & \mathrm{CP}=\lrcorner \end{aligned}$ | $V_{C C}=M A X$ |

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS

| Symbol | Parameter |  |  |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ \mathrm{v}_{\mathrm{CC}}=+5.0 \mathrm{~V} \\ \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{gathered}$ |  | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=0 \text { to }+70^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{C}}=5.0 \mathrm{~V} \pm 10 \% \\ \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{gathered}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $\mathrm{f}_{\text {max }}$ | Maximum Shift Frequency | 105 |  | 90 |  | MHz |
| $\begin{aligned} & \hline \text { tPLH } \\ & \text { tpHL } \end{aligned}$ | Propagation Delay CP to $Q_{n}$ | $\begin{aligned} & 3.0 \\ & 3.5 \end{aligned}$ | $\begin{aligned} & 7.0 \\ & 7.5 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 3.5 \end{aligned}$ | $\begin{aligned} & 8.0 \\ & 8.0 \end{aligned}$ | ns |
| tPHL | Propagation Delay MR to $Q_{n}$ | 4.5 | 12 | 4.5 | 14 | ns |

AC OPERATING REQUIREMENTS

| Symbol | Parameter |  |  |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}}=+5.0 \mathrm{~V} \end{gathered}$ |  | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=0 \text { to }+70^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{C}}=5.0 \mathrm{~V} \pm 10 \% \end{gathered}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $\begin{aligned} & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\ & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \end{aligned}$ | Set up Time, HIGH or LOW $\mathrm{P}_{\mathrm{n}}$ or $\mathrm{D}_{\mathrm{SR}}$ or $\mathrm{D}_{\mathrm{SL}}$ to CP | $\begin{aligned} & 4.0 \\ & 4.0 \end{aligned}$ |  | $\begin{aligned} & 4.0 \\ & 4.0 \end{aligned}$ |  | ns |
| $\begin{aligned} & \mathrm{t}_{\mathrm{h}}(\mathrm{H}) \\ & \mathrm{t}_{\mathrm{h}}(\mathrm{~L}) \end{aligned}$ | Hold Time, HIGH or LOW $P_{n}$ or DSR or DSL to CP | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ |  |  |
| $\begin{aligned} & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\ & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \end{aligned}$ | Set up Time, HIGH or LOW $S_{n}$ to CP | $\begin{aligned} & 8.0 \\ & 8.0 \end{aligned}$ |  | $\begin{aligned} & 9.0 \\ & 8.0 \end{aligned}$ |  | ns |
| $\begin{aligned} & \mathrm{t}_{\mathrm{h}}(\mathrm{H}) \\ & \mathrm{th}_{\mathrm{h}}(\mathrm{~L}) \end{aligned}$ | Hold Time, HIGH or LOW $S_{n}$ to CP | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  |  |
| $\mathrm{t}_{\mathrm{w}}(\mathrm{H})$ | CP Pulse Width HIGH | 5.0 |  | 5.5 |  | ns |
| $\mathrm{t}_{\mathrm{w}}(\mathrm{L})$ | MR Pulse Width LOW | 5.0 |  | 5.0 |  | ns |
| $t_{\text {rec }}$ | Recovery Time MR to CP | 7.0 |  | 8.0 |  | ns |

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