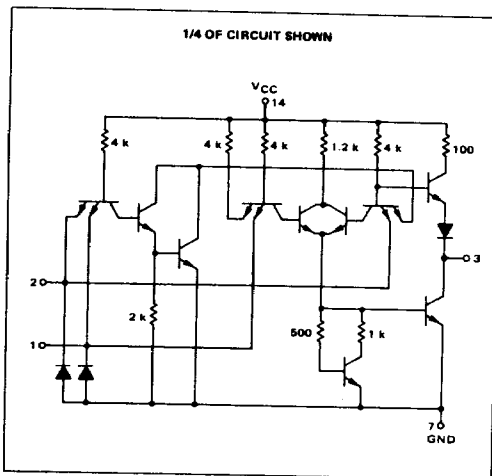


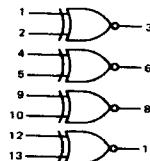
QUAD 2-INPUT
EXCLUSIVE "NOR" GATE

MTTL III MC3100/3000 series

MC3122F • MC3022F
MC3122L • MC3022L,P



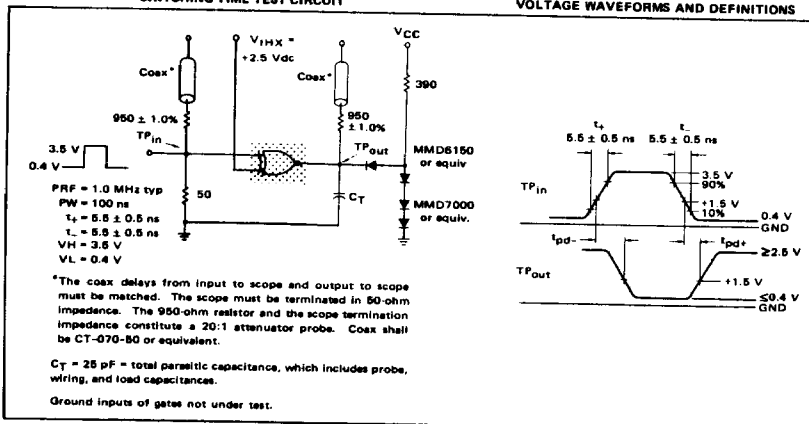
This device consists of four 2-input Exclusive NOR gates. They can be used to build parity checking/generating functions. Up/down counters can be built using these gates and J-K flip-flops.



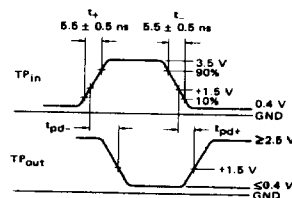
Positive Logic: $3 = \bar{1} \cdot \bar{2} + 1 \cdot 2$

Input Loading Factor = 1.6
Output Loading Factor = 8
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 14 ns typ

SWITCHING TIME TEST CIRCUIT



VOLTAGE WAVEFORMS AND DEFINITIONS

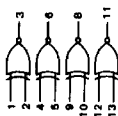


See General Information section for packaging.

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ELECTRICAL CHARACTERISTICS

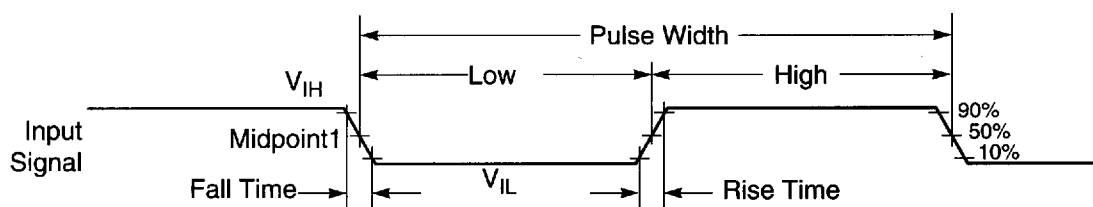
Test procedures are shown for only one gate. The other gates is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic		TEST CURRENT/VOLTAGE VALUES												TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												Good																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
		mA						Volts																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																											
Symbol	Units	-55°C			+25°C			+75°C			0°C			+55°C			+75°C			I _{CC}	I _{ON}	I _{OP}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC}	V _{OC}	V _{CC}	V _{OC}	V _{IN}	V _{IP}	V _{IN}	V _{IP}	V _{CC} </

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, RESET, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference