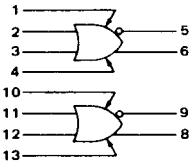


MC1024
MC1224

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

Expandable inputs are available on pins 1, 4 and 10, 13 as shown in the circuit schematic.

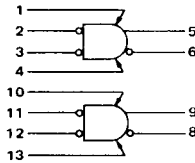
POSITIVE LOGIC



$$5 = \overline{2 + 3}$$

$$6 = 2 + 3$$

NEGATIVE LOGIC

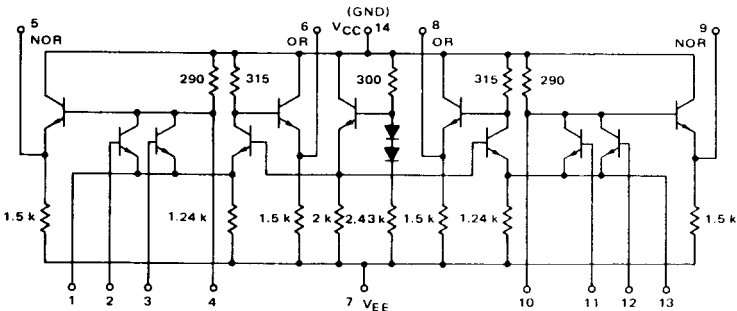


$$5 = \overline{2 \cdot 3}$$

$$6 = 2 \cdot 3$$

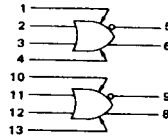
DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 95 mW typical

CIRCUIT SCHEMATIC



MC1024, MC1224 (continued)

ELECTRICAL CHARACTERISTICS



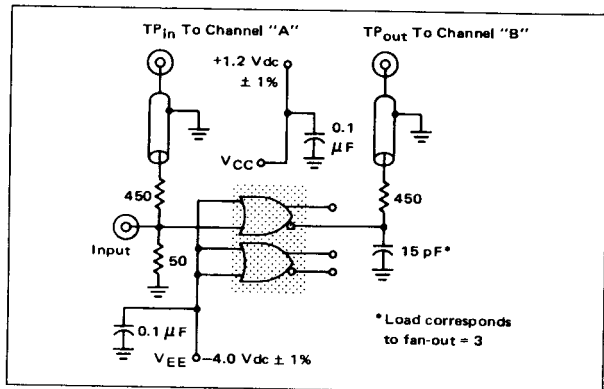
Test procedures are shown for only one gate.
The other gate is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1224 Test Limits						MC1024 Test Limits										
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C		Unit				
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max					
Power Supply Drain Current	I_E	7	-	-	-	26	-	-	-	-	-	-	-	-	-	mAdc			
Input Current	I_{in}	2 3	-	-	-	100 100	-	-	-	-	-	-	100 100	-	-	μ Adc			
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	-	-	-	-	0.2	-	1.0	μ Adc			
"NOR" Logical "1" Output Voltage	V_{OH1}	5 5	-0.990 -0.990	-0.825 -0.825	-0.850 -0.850	-0.700 -0.700	-0.700 -0.700	-0.530 -0.530	Vdc	-0.895 -0.895	-0.740 -0.740	-0.850 -0.850	-0.700 -0.700	-0.775 -0.775	-0.615 -0.615	Vdc			
"NOR" Logical "0" Output Voltage	V_{OL}	5 5	-1.890 -1.890	-1.580 -1.580	-1.800 -1.800	-1.500 -1.500	-1.720 -1.720	-1.380 -1.380	Vdc	-1.830 -1.830	-1.525 -1.525	-1.800 -1.800	-1.500 -1.500	-1.760 -1.760	-1.435 -1.435	Vdc			
"OR" Logical "1" Output Voltage	V_{OH1}	6 6	-0.990 -0.990	-0.825 -0.825	-0.850 -0.850	-0.700 -0.700	-0.700 -0.700	-0.530 -0.530	Vdc	-0.895 -0.895	-0.740 -0.740	-0.850 -0.850	-0.700 -0.700	-0.775 -0.775	-0.615 -0.615	Vdc			
"OR" Logical "0" Output Voltage	V_{OL}	6 6	-1.890 -1.890	-1.580 -1.580	-1.800 -1.800	-1.500 -1.500	-1.720 -1.720	-1.380 -1.380	Vdc	-1.830 -1.830	-1.525 -1.525	-1.800 -1.800	-1.500 -1.500	-1.760 -1.760	-1.435 -1.435	Vdc			
Switching Times Propagation Delay (Fan-Out = 3)			Typ		Max		Typ		Max		Typ		Max		Typ		Max		
			t_{2-5-}	5	5.0	7.0	5.0	7.0	6.5	9.0	ns	5.0	7.0	5.0	7.0	6.0	8.0	ns	
			t_{2-5+}	5	4.0	7.5	4.0	7.5	5.5	9.0	ns	4.0	7.5	4.0	7.5	5.0	8.5	ns	
			t_{2-6-}	6	4.0	7.5	4.0	7.0	5.5	8.5		4.0	7.0	4.0	7.0	5.0	8.0		
			t_{2-6+}	6	4.0	7.0	4.0	7.0	5.5	9.0		4.0	7.0	4.0	7.0	5.0	8.0		
			(Fan-Out = 15)	t_{2-5-}	5	14	-	14	-	18		-	14	-	14	-	16		-
			t_{2-5+}	5	5.0	-	5.0	-	7.0	-		5.0	-	5.0	-	6.0	-		
			t_{2-6-}	6	6.0	-	6.0	-	8.0	-		6.0	-	6.0	-	7.0	-		
			t_{2-6+}	6	13	-	13	-	17	-		13	-	13	-	15	-		
			Rise Time (Fan-Out = 3)	t_{5+}	5	5.0	7.5	5.0	7.5	6.0		9.0	5.0	7.5	5.0	7.5	5.0		8.0
			t_{6+}	6	4.0	7.0	4.0	6.5	5.5	8.0		4.0	6.5	4.0	6.5	5.0	7.0		
			Fall Time (Fan-Out = 3)	t_{5-}	5	5.0	8.5	5.0	8.0	6.0		10	5.0	8.0	5.0	8.0	5.5		9.0
t_{6-}	6	5.0	8.0	5.0	8.0	7.0	10	5.0	8.0	5.0		8.0	6.0	9.0					

* Individually test each input using the pin connections shown.

† V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

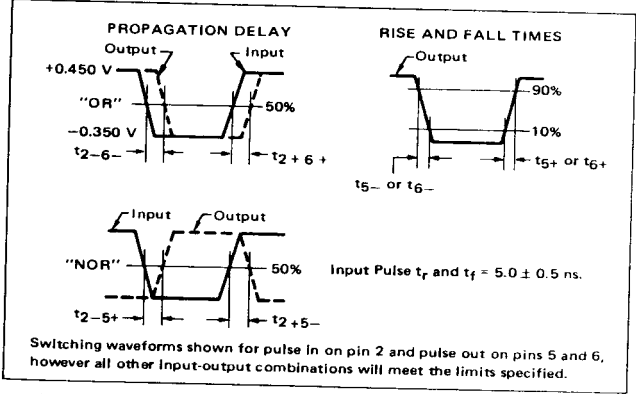
SWITCHING TIME TEST CIRCUIT @ 25°C



@Test
Temperature
MC1224
-55°C
+25°C
+125°C
MC1024
0°C
+25°C
+75°C

TEST VOLTAGE/CURRENT VALUES				
V _{dc} = 1.0 V _{cc}				
V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L mAdc
-5.2 to -1.405	-1.165 to 0.825	-	-5.2	-2.5
-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					V _{CC} (Gnd)
			V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L	
Power Supply Drain Current	I _E	7	-	-	-	2, 3, 7, 11, 12	-	14
Input Current	I _{in}	2 3	-	-	2 3	3, 7, 11, 12	-	14
Input Leakage Current	I _R	Inputs*	-	-	-	2, 3, 7, 11, 12	-	14
"NOR" Logical "1" Output Voltage	V _{OH} †	5 5	2 3	-	-	3, 7, 11, 12	5 5	14 14
"NOR" Logical "0" Output Voltage	V _{OL}	5 5	-	2 3	-	3, 7, 11, 12	-	14 14
"OR" Logical "1" Output Voltage	V _{OH} †	6 6	-	2 3	-	3, 7, 11, 12	-	14 14
"OR" Logical "0" Output Voltage	V _{OL}	6 6	2 3	-	-	3, 7, 11, 12	6 6	14 14
Switching Times								
Propagation Delay (Fan-Out = 3)			Pulse In		Pulse Out		V _{EE} = -4.0 Vdc	(+12 V)
	t ₂₊₅₋	5	2	5	-	3, 7, 11, 12	-	14
	t ₂₋₅₊	5	-	5	-	-	-	-
	t ₂₊₆₊	6	-	6	-	-	-	-
	t ₂₋₆₋	6	-	6	-	-	-	-
(Fan-Out = 15)	t ₂₊₅₋	5	-	5	-	-	-	-
	t ₂₋₅₊	5	-	5	-	-	-	-
	t ₂₊₆₊	6	-	6	-	-	-	-
	t ₂₋₆₋	6	-	6	-	-	-	-
Rise Time (Fan-Out = 3)	t ₅₋	5	-	5	-	-	-	-
	t ₆₋	6	-	6	-	-	-	-
Fall Time (Fan-Out = 3)	t ₅₊	5	-	5	-	-	-	-
	t ₆₊	6	-	6	-	-	-	-



SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

The MC1024/MC1224 dual 2-input expandable OR/NOR gate provides the capability of increasing fan-in by making available the collector and emitter nodes of the standard gate. Note that complementary outputs are available, lending to circuit flexibility. By using the MC1025/MC1225 expander 6, 7, 10, 11, 12, 15, 16, or 20 gate inputs may be obtained with one or two expanders per gate. Note that as fan-in is increased, capacitance is added to the input collector node and propagation delays through the gate will increase. A maximum fan-in of 20 is recommended for high-speed operation. If high speed is not required, larger fan-ins may be utilized.

The expandable inputs allow a large fan-in NOR or NAND gate to be obtained, where power dissipation is decreased at the expense of propagation delay. The OR propagation delay times vary little with increasing fan-in since capacitance is not being added to the OR collector node. At a fan-in of 20, NOR output rise and fall times approach 20 ns, while OR output rise and fall times remain about 4.0 ns. For minimal added capacitance at the NOR collector node, lead lengths should be kept short and the circuits wired in directly rather than using sockets. Typical propagation delay curves versus fan-in and temperature are shown below.

TYPICAL PROPAGATION DELAY TIMES

