

FEATURES:

- 5Ω A/B bi-directional switch
- Isolation Under Power-Off Conditions
- Over-voltage tolerant
- Latch-up performance exceeds 100mA
- Vcc = 2.3V - 3.6V, normal range
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- Available in TSSOP package

APPLICATIONS:

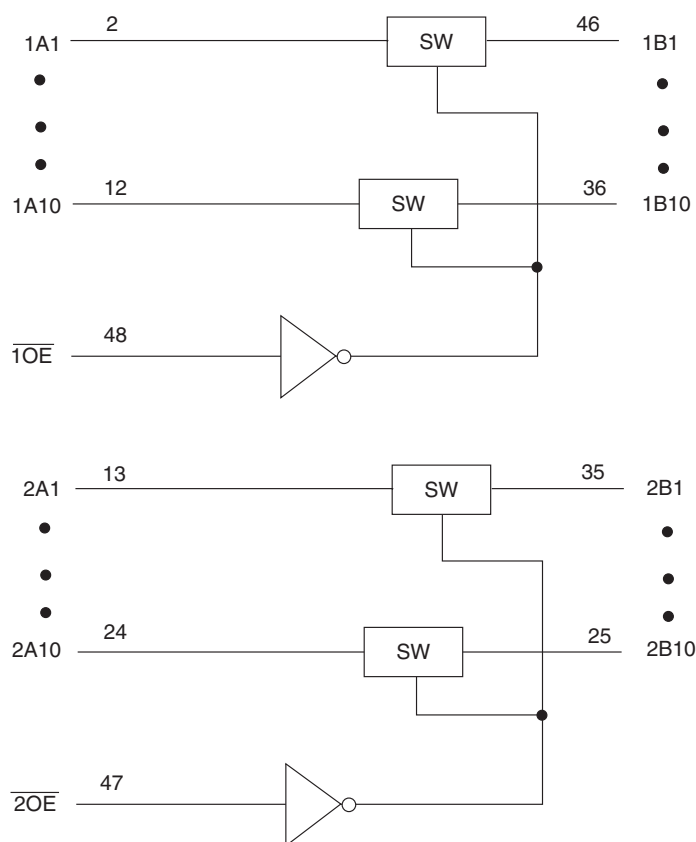
- 3.3V High Speed Bus Switching and Bus Isolation

DESCRIPTION:

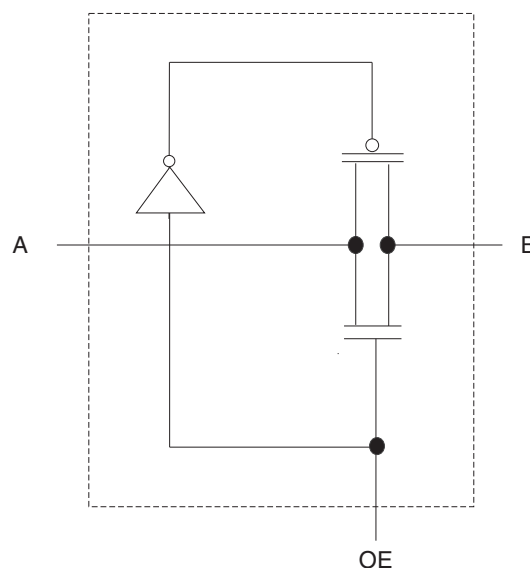
The CBTLV16210 operates as a single 20-bit bus switch or as a dual 10-bit bus switch, which provides high-speed switching. This device has very low ON resistance, resulting in under 250ps propagation delay through the switch. When Output Enable ($\overline{OE}$) is low, the corresponding 10-bit bus switch is on and port A is connected to Port B. When $\overline{OE}$ is high, the switch is off and a high impedance exists between Port A and Port B.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to Vcc through a pullup resistor.

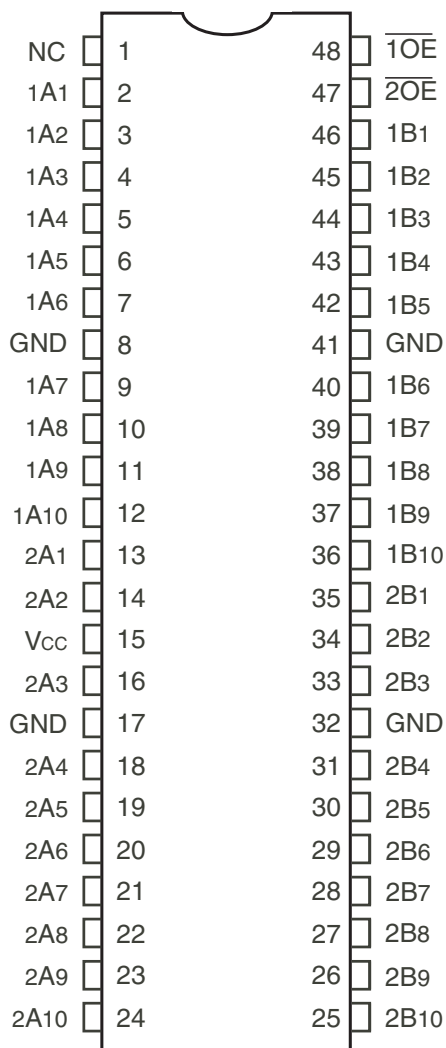
FUNCTIONAL BLOCK DIAGRAM



SIMPLIFIED SCHEMATIC, EACH SWITCH



PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
TSSOP	PAG48	PAG

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{CC}	Supply Voltage Range	−0.5 to 4.6	V
V _I	Input Voltage Range	−0.5 to 4.6	V
	Continuous Channel Current	128	mA
I _{IK}	Input Clamp Current, V _{I/O} < 0	−50	mA
T _{STG}	Storage Temperature Range	−65 to +150	°C

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Names	Description
$\overline{xOE}$	Output Enable (Active LOW)
xAx	Port A Inputs or Outputs
xBx	Port B Inputs or Outputs

FUNCTION TABLE⁽¹⁾

Input	Operation
$\overline{OE}$	
L	A-Port = B-Port
H	Disconnect

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level

OPERATING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{CC}	Supply Voltage		2.3	3.6	V
V _{IH}	High-Level Control Input Voltage	V _{CC} = 2.3V to 2.7V	1.7	—	V
		V _{CC} = 2.7V to 3.6V	2	—	
V _{IL}	Low-Level Control Input Voltage	V _{CC} = 2.3V to 2.7V	—	0.7	V
		V _{CC} = 2.7V to 3.6V	—	0.8	
T _A	Operating Free-Air Temperature		−40	+85	°C

NOTE:

- All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IK}	Control Inputs, Data I/O	V _{CC} = 3V, I _I = -18mA		—	—	-1.2	V
I _I	Control Inputs	V _{CC} = 3.6V, V _I = V _{CC} or GND		—	—	±1	μA
I _{OZ}	Data I/O	V _{CC} = 3.6V, V _O = 0V or 3.6V switch disabled		—	—	5	μA
I _{OFF}		V _{CC} = 0V, V _I or V _O = 0V or 3.6V		—	—	10	μA
I _{CC}		V _{CC} = 3.6V, I _O = 0, V _I = V _{CC} or GND		—	—	10	μA
ΔI _{CC} ⁽²⁾	Control Inputs	V _{CC} = 3.6V, one input at 3V, other inputs at V _{CC} or GND		—	—	300	μA
C _I	Control Inputs	V _I = 3V or 0		—	4	—	pF
C _{IO(OFF)}		V _O = 3V or 0, $\overline{OE}$ = V _{CC}		—	6.5	—	pF
R _{ON} ⁽³⁾	Max. at V _{CC} = 2.3V Typ. at V _{CC} = 2.5V	V _I = 0	I _O = 64mA	—	5	8	Ω
			I _O = 24mA	—	5	8	
	V _{CC} = 3V	V _I = 1.7V	I _O = 15mA	—	27	40	
		V _I = 0	I _O = 64mA	—	5	7	
			I _O = 24mA	—	5	7	
		V _I = 2.4V	I _O = 15mA	—	10	15	

NOTES:

- Typical values are at 3.3V, +25°C ambient.
- The increase in supply current is attributable to each input that is at the specified voltage level rather than V_{CC} or GND.
- This is measured by the voltage drop between the A and B terminals at the indicated current through the switch.

SWITCHING CHARACTERISTICS

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
t _{PD} ⁽¹⁾	Propagation Delay A to B or B to A	—	0.15	—	0.25	ns
t _{EN}	Output Enable Time $\overline{OE}$ to A or B	1	6.8	1	6	ns
t _{DIS}	Output Disable time $\overline{OE}$ to A or B	1	7.3	1	7.4	ns

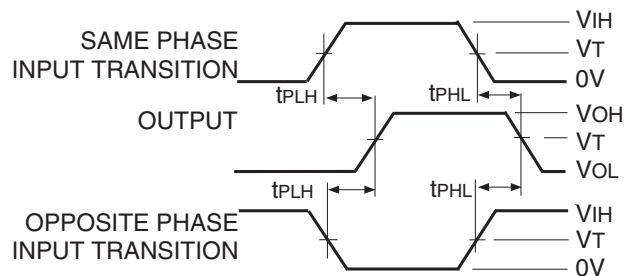
NOTE:

- The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

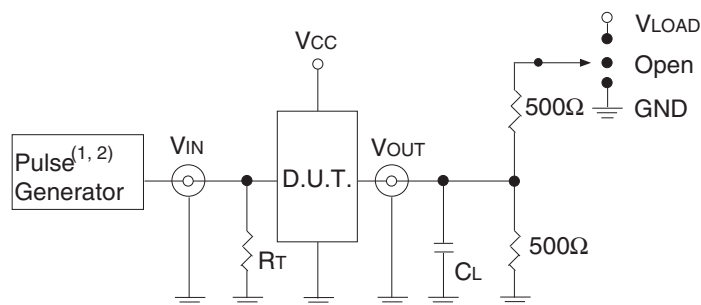
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	$2 \times V_{CC}$	$2 \times V_{CC}$	V
V_{IH}	3	V_{CC}	V
V_T	1.5	$V_{CC} / 2$	V
V_{LZ}	300	150	mV
V_{HZ}	300	150	mV
C_L	50	30	pF



Propagation Delay



Test Circuits for All Outputs

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

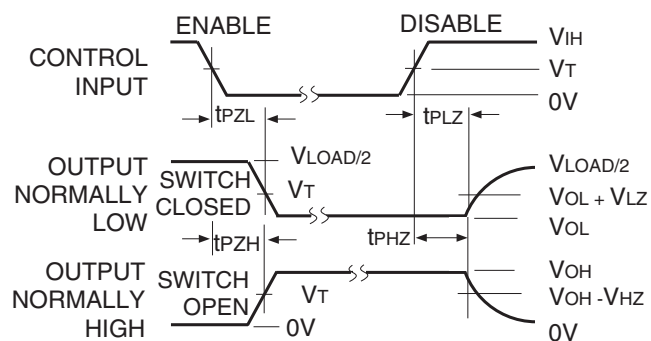
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.
2. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_r \leq 2\text{ns}$; $t_f \leq 2\text{ns}$.

SWITCH POSITION

Test	Switch
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND
t_{PD}	Open

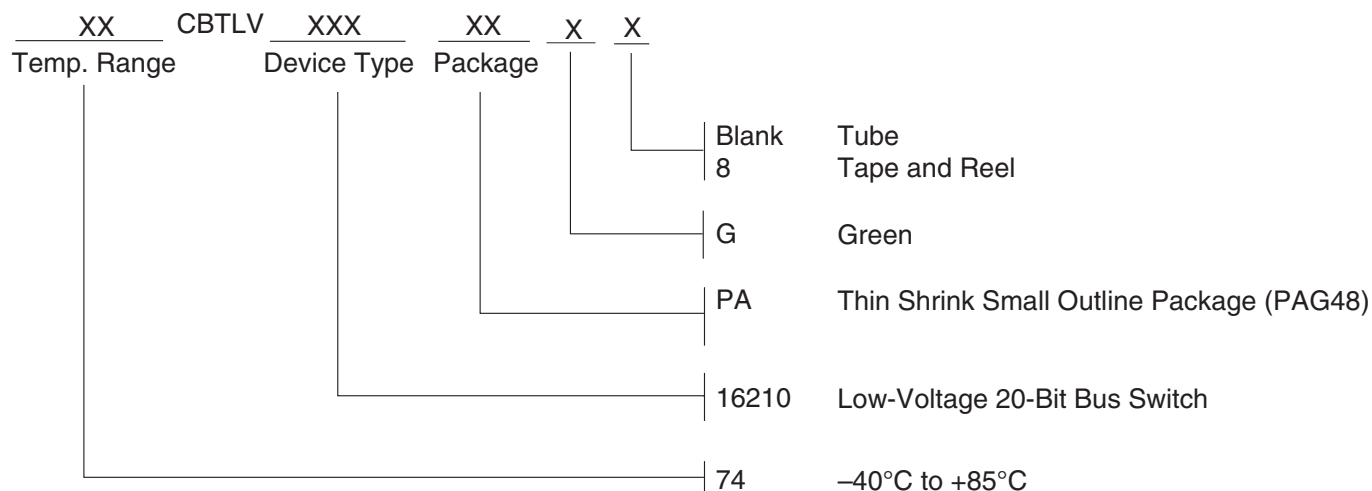


NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times

ORDERING INFORMATION



Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
	74CBTLV16210PAG	PAG48	TSSOP	I
	74CBTLV16210PAG8	PAG48	TSSOP	I

Datasheet Document History

12/01/2014	Pg. 5	Updated the ordering information by adding Tape and Reel information.
06/03/2019	Pg. 2,5	Added table under pin configuration diagram with detailed package information and orderable part information table. Updated the ordering information diagram in clearer detail.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.