

MC100LVEL56

3.3 V ECL Dual Differential 2:1 Multiplexer

Description

The MC100LVEL56 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals.

The device features both individual and common select inputs to address both data path and random logic applications.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to V_{EE} . The $\bar{D}$ input will bias around $V_{CC}/2$ forcing the Q output LOW.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

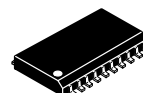
Features

- 580 ps Typical Propagation Delays
- Separate and Common Select
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:
 $V_{CC} = 3.0$ V to 3.8 V with $V_{EE} = 0$ V
- NECL Mode Operating Range:
 $V_{CC} = 0$ V with $V_{EE} = -3.0$ V to -3.8 V
- Internal Input Pulldown Resistors on D(s), SEL(s), and COM_SEL
- Q Output will Default LOW with Inputs Open or at V_{EE}
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



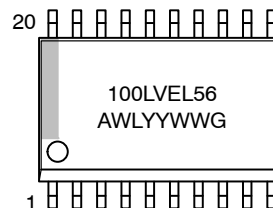
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SOIC-20 WB
DW SUFFIX
CASE 751D

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

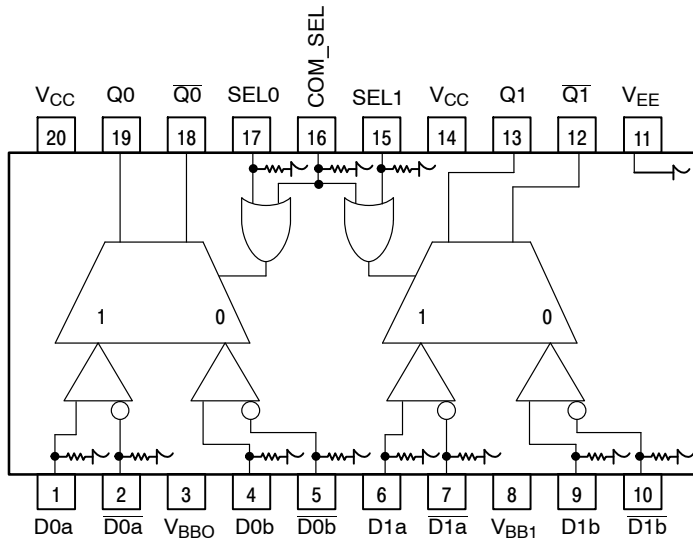
*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
MC100LVEL56DWG	SOIC-20 WB (Pb-Free)	38 Units/Tube
MC100LVEL56DWR2G	SOIC-20 WB (Pb-Free)	1000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Package (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D0a* – D1a*	ECL Input Data a
D0a* – D1a*	ECL Input Data a Invert
D0b* – D1b*	ECL Input Data b
D0b* – D1b*	ECL Input Data b Invert
SEL0* – SEL1*	ECL Indiv. Select Input
COM_SEL*	ECL Common Select Input
V_{BB0} , V_{BB1}	Output Reference Voltage
Q0 – Q1	ECL True Outputs
$\bar{Q}0$ – $\bar{Q}1$	ECL Inverted Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default LOW when left open.

Table 2. TRUTH TABLE

SEL0	SEL1	COM_SEL	Q0, $\bar{Q}0$	Q1, $\bar{Q}1$
X	X	H	a	a
L	L	L	b	b
L	H	L	b	a
H	H	L	a	a
H	L	L	a	b

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 K Ω
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Device Model	> 2 kV > 200 V > 4 kV
Moisture Sensitivity, (Note 1) Pb-Free	Level 3
Flammability Rating Oxygen Index	UL 94 V-0 @ 0.125 in 28 to 34
Transistor Count	147
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

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Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8 to 0	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		–8 to 0	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 to 0 –6 to 0	V
I _{out}	Output Current	Continuous Surge		50 100	mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			–40 to +85	°C
T _{stg}	Storage Temperature Range			–65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC–20 WB	90 60	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC–20 WB	30 to 35	°C/W
T _{sol}	Wave Solder (Pb-Free)	< 2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. LVPECL DC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0.0 V (Note 1))

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		20	24		20	24		20	24	mA
V _{OH}	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V _{OL}	Output LOW Voltage (Note 2)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V _{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
V _{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3) V _{pp} < 500 mV V _{pp} ≥ 500 mV	1.3 1.5		2.9 2.9	1.2 1.4		2.9 2.9	1.2 1.4		2.9 2.9	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current Dn Dn	0.5 –600			0.5 –600			0.5 –600			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} – 2.0 V.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{pp}(min) and 1 V.

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Table 6. LVNECL DC CHARACTERISTICS ($V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		20	24		20	24		20	24	mA
V_{OH}	Output HIGH Voltage (Note 2)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage (Note 2)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{BB}	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3) $V_{pp} < 500\text{ mV}$ $V_{pp} \geq 500\text{ mV}$	-2.0 1.8		-0.4 0.4	-2.1 1.9		-0.4 0.4	-2.1 1.9		-0.4 0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D_n $\overline{D_n}$	0.5 -600			0.5 -600			0.5 -600			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V .

Table 7. AC CHARACTERISTICS ($V_{CC} = 3.3\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (See Figure 2, $F_{max/JITTER}$)					1					GHz
t_{PLH} t_{PHL}	Propagation Delay to Output D SEL COMSEL	400 430 430		600 730 730	420 440 440		620 740 740	440 450 450		640 750 750	ps
t_{SKEW}	Within-Device Skew (Note 2)		40	80		40	80		40	80	ps
t_{SKEW}	Duty Cycle Skew (Note 3)			100			100			100	ps
t_{JITTER}	Random Clock Jitter (RMS)					1.5					ps
V_{PP}	Input Swing (Note 4)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	200		540	200		540	200		540	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. V_{EE} can vary $\pm 0.3\text{ V}$.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
4. $V_{pp(min)}$ is minimum input swing for which AC parameters are guaranteed.

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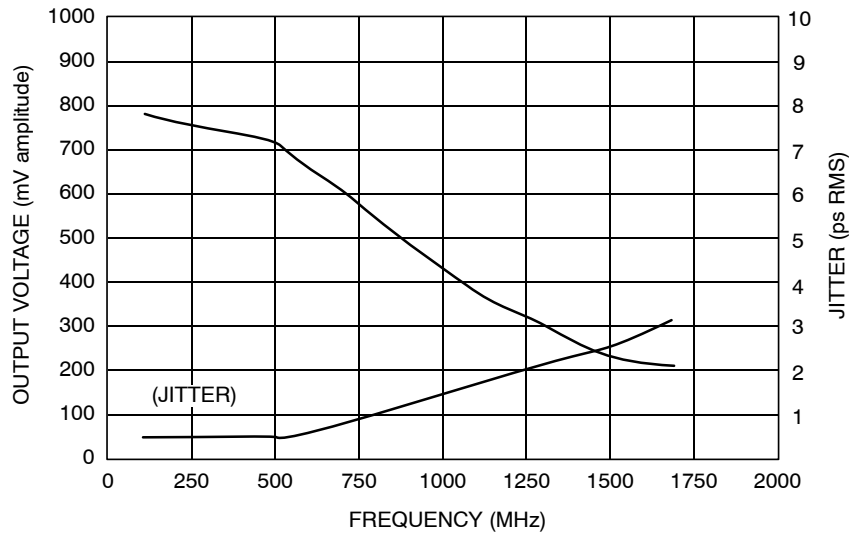


Figure 2. $F_{\max}$ /Jitter

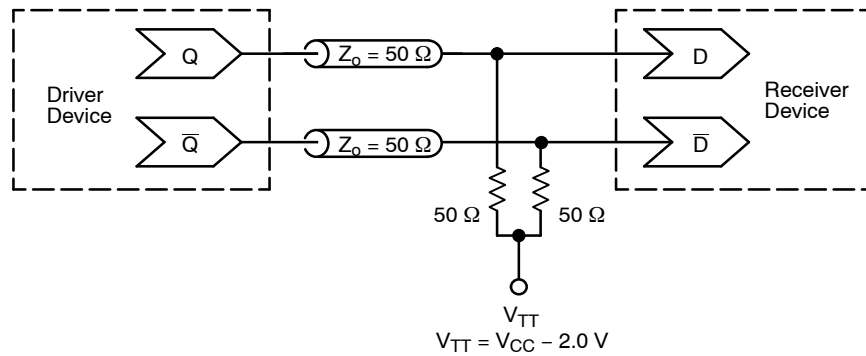


Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

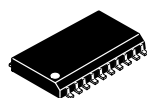
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

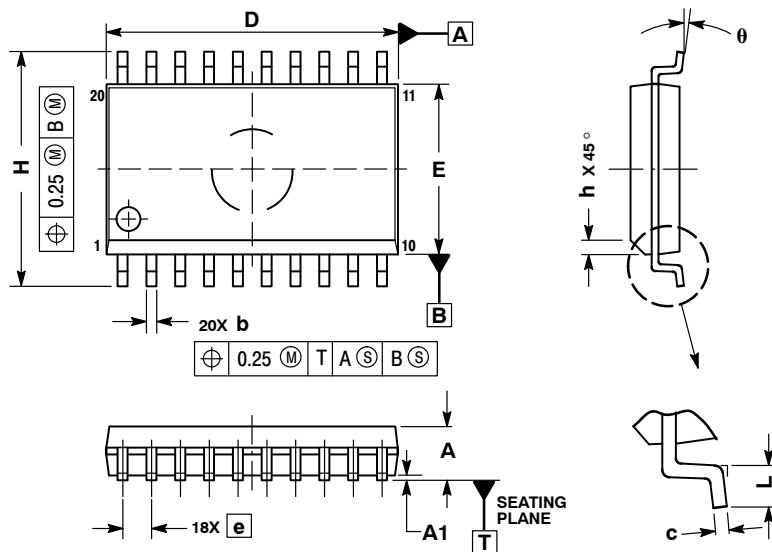
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SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

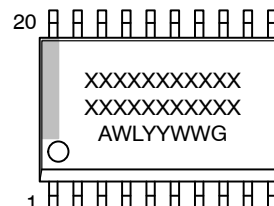


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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