



Integrated Device Technology, Inc.

QUAD 2:1 MUX/DEMUX BUS SWITCH

IDT74FST3257
PRELIMINARY

FEATURES:

- Bus switches provide zero delay paths
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- Low switch on-resistance:
FST3xxx – 5Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- Available in QSOP and SOIC

DESCRIPTION:

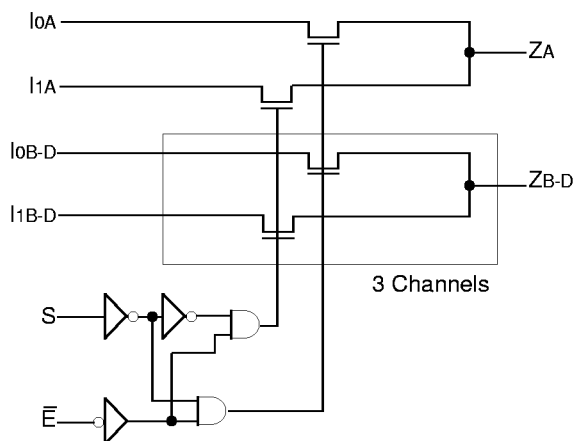
The FST3257 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source

capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts or the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

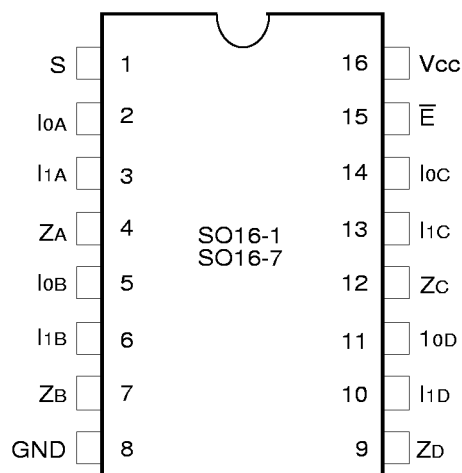
The FST3257 provides a 4-bit 2:1 multiplexer/demultiplexer. The S pin controls the mux select and the $\bar{E}$ pin serves as the switch enable.

FUNCTIONAL BLOCK DIAGRAM



3257 drw 01

PIN CONFIGURATION



SOIC/QSOP
TOP VIEW

3257 drw 02

PIN DESCRIPTION

Pin Names	I/O	Description
I0A-I0D	I/O	Port 0
I1A-I1D	I/O	Port 1
$\bar{E}$	I	Switch Enable (Active Low)
S	I	Mux Select
ZA-ZB	I/O	Port Z

3257 tbl 01

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COMMERCIAL TEMPERATURE RANGES

AUGUST 1996

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
TSTG	Storage Temperature	−65 to +150	°C
IOUT	Maximum Continuous Channel Current	128	mA

NOTES: 3257 tbl 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc, Control and Switch terminals.

FUNCTION TABLE⁽¹⁾

$\bar{E}$	S	I0A-D	I1A-D	ZA-D
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

NOTE:

3257 tbl 03

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Typ.	Unit
CIN	Control Input Capacitance		4	pF
Ci/O	Switch Input/Output Capacitance	Switch Off		pF

NOTES:

3257 tbl 04

- Capacitance is characterized but not tested
- TA = 25°C, f = 1MHz, VIN = 0V, VOUT = 0V

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = −40°C to +85°C, Vcc = 5.0V ±5%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
VIH	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V
VIL	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
IiH	Input HIGH Current	Vcc = Max. Vi = Vcc	—	—	±1	μA
IiL	Input LOW Current		—	—	±1	
IOZH	High Impedance Output Current	Vcc = Max. Vo = Vcc	—	—	±1	μA
IOZL	(3-State Output pins)		—	—	±1	
Ios	Short Circuit Current	Vcc = Max., Vo = GND ⁽³⁾	—	300	—	mA
VIK	Clamp Diode Voltage	Vcc = Min., IIN = −18mA	—	−0.7	−1.2	V
RON	Switch On Resistance ⁽⁴⁾	Vcc = Min., VIN = 0.0V, ION = 30mA	—	5	7	Ω
		Vcc = Min., VIN = 2.4V, ION = 15mA	—	10	15	Ω
IOFF	Input/Output Power Off Leakage	Vcc = 0V, VIN or Vo ≤ 4.5V	—	—	±1	μA
ICC	Quiescent Power Supply Current	Vcc = Max., Vi = GND or Vcc	—	0.1	3	μA

NOTES:

3257 tbl 05

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at Vcc = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open Enable Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	30	40	$\mu\text{A}/$ MHz/ Switch
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open Enable Pin Toggling (4 Switches Toggling) $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.2	1.6	mA
			$V_{IN} = 3.4$ $V_{IN} = \text{GND}$	—	1.5	2.4	

NOTES:

3257 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HT} + I_{CCD} (f_i N)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_i = \text{Input Frequency}$
 $N = \text{Number of Switches Toggling at } f_i$
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0V \pm 5\%$

Symbol	Description	Condition ⁽¹⁾	Min. ⁽²⁾	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay I to Z, Z to I ^(3,4)	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	—	0.25	ns
t_{PLH} t_{PHL}	Switch Multiplex Delay S to I, Z		1.5	—	5.2	ns
t_{PZH} t_{PZL}	Switch Turn on Delay $\bar{E}$ to I, Z		1.5	—	4.8	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay $\bar{E}$ to I, Z ⁽³⁾		1.5	—	5.0	ns
$ Q_{CI} $	Charge Injection, Typical ^(5,6)		—	1.5	—	pC
$ Q_{CDI} $	Charge Injection, Typical ^(6,7)		—	0.5	—	pC

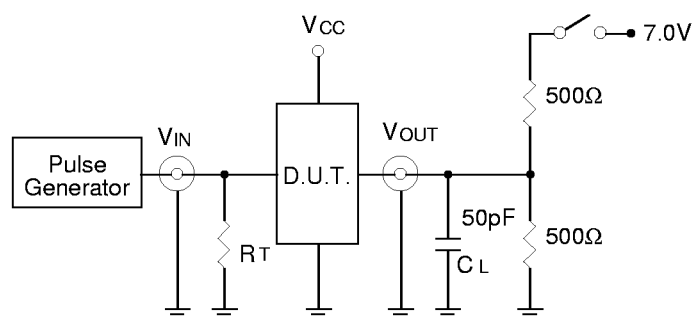
NOTES:

3257 tbl 07

- See test circuit and waveforms.
- Minimum limits guaranteed but not tested.
- This parameter is guaranteed by design but not tested.
- The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- Measured at switch turn off, load = 50 pF in parallel with 10 m Ω scope probe, $V_{IN} = 0.0$ volts.
- Measured at switch turn off through bus multiplexer, (e.g. - I₀ to Z => I₁ to Z), load = 50 pF in parallel with 10 M Ω scope probe, V_{IN} at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the I₀ to Z switch is compensated by the turn on of the I₁ to Z switch.
- Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3257 Ink 03

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

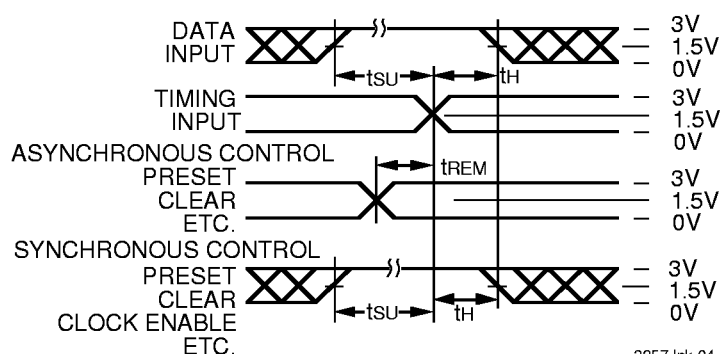
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

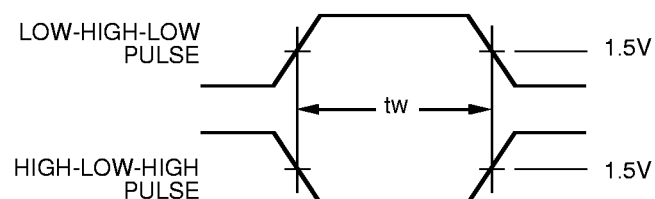
3257 Ink 08

SET-UP, HOLD AND RELEASE TIMES



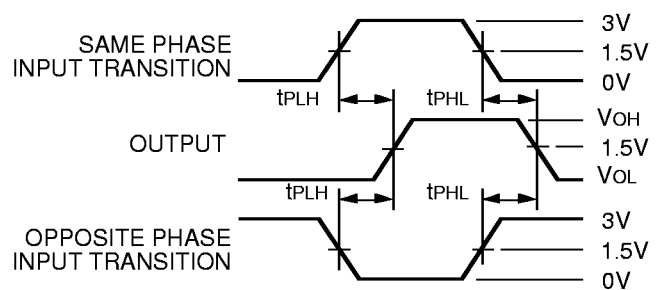
3257 Ink 04

PULSE WIDTH



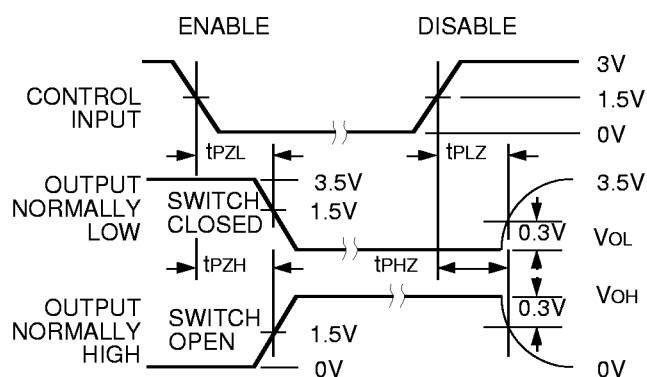
3257 Ink 03

PROPAGATION DELAY



3257 Ink 06

ENABLE AND DISABLE TIMES

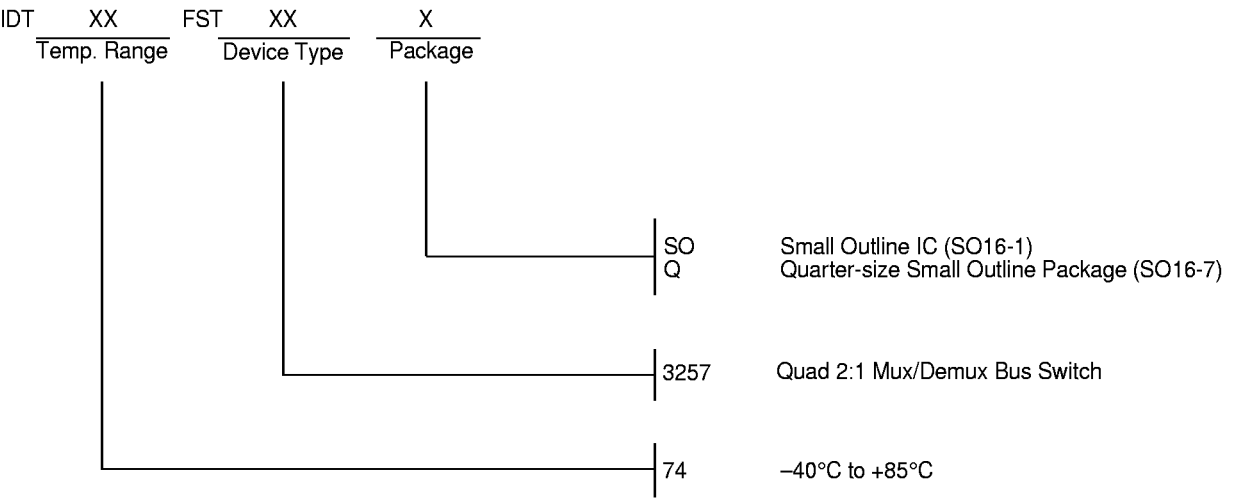


3257 Ink 07

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$

ORDERING INFORMATION

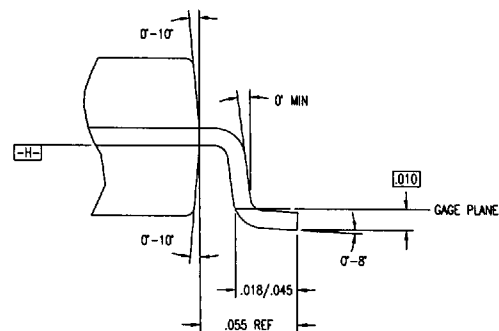
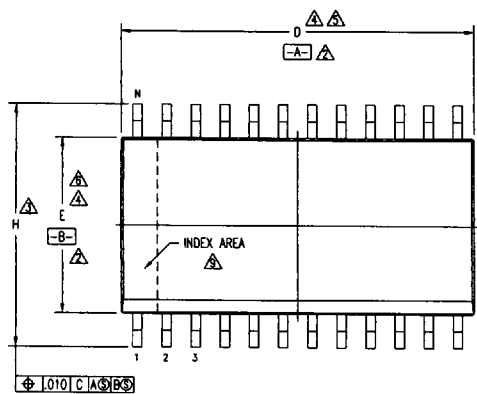


3257 drw 08

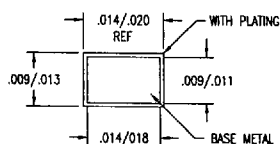
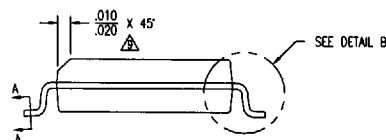
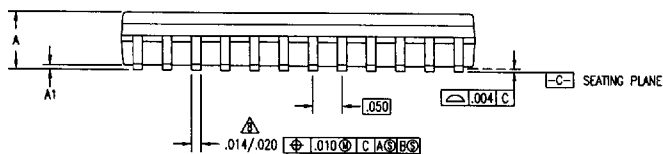
PACKAGE DIAGRAM OUTLINES

SOIC

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27843	06	REDRAW TO JEDEC FORMAT	03/15/95	



DETAIL B



SECTION A-A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Slender Way, Santa Clara, CA 95054 PHONE: (408) 727-8116 FAX: (408) 482-8874 TWR: 910-338-2070	
DECIMAL	ANGULAR	DATE	03/15/95
XX±	±	TITLE	PS PACKAGE OUTLINE
XXX±		SIZE	.300" BODY WIDTH SOIC
XXXX±		CHECKED	.050" PITCH
APPROVALS	DATE	SIZE	DRAWING No.
DRN	03/15/95	C	PSC-4007
CHECKED		REV	06
DO NOT SCALE DRAWING			

PACKAGE DIAGRAM OUTLINES SOIC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27643	06	REDRAW TO JEDEC FORMAT	03/15/95	

SYMBOL	DWG #		S016-1		NOTE	DWG #		S018-1		NOTE	DWG #		S020-2		NOTE	DWG #		S024-2		NOTE	DWG #		S028-2		NOTE
	JEDEC VARIATION			JEDEC VARIATION		JEDEC VARIATION			JEDEC VARIATION			JEDEC VARIATION													
	AA			AB		AC			AD			AE													
	MIN	NOM	MAX	MIN		NOM	MAX	MIN	NOM		MAX	MIN	NOM	MAX		MIN	NOM	MAX							
A	.095	.100	.104		.095	.100	.104		.095	.100	.104		.095	.100	.104		.095	.100	.104		.095	.100	.104		
A1	.005	.008	.012		.005	.008	.012		.005	.008	.012		.005	.008	.012		.005	.008	.012		.005	.008	.012		
D	.403	.408	.413	4,5	.447	.454	.462	4,5	.497	.504	.511	4,5	.600	.607	.614	4,5	.700	.706	.712	4,5	.700	.706	.712	4,5	
E	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6	
H	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3	
N	16				18				20				24				28								

NOTES:

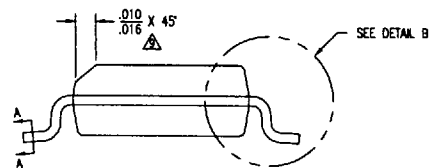
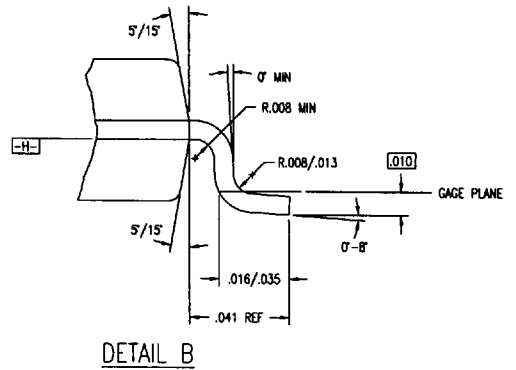
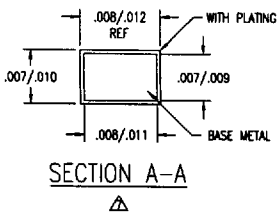
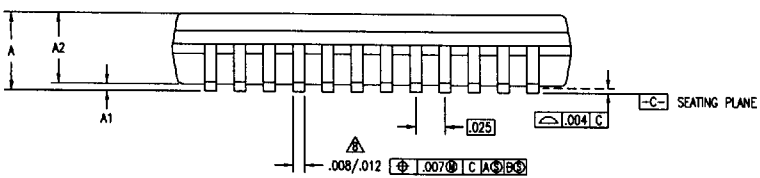
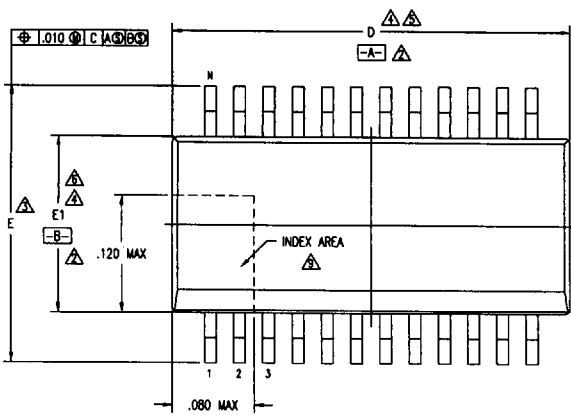
- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- △ DATUMS ☐-A- and ☐-B- TO BE DETERMINED AT DATUM PLANE ☐-H-
- △ DIMENSION H TO BE DETERMINED AT SEATING PLANE ☐-C-
- △ DIMENSIONS D AND E ARE TO BE DETERMINED AT DATUM PLANE ☐-H-
- △ DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- △ DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- △ LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- △ THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- 10 ALL DIMENSIONS ARE IN INCHES
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-013, VARIATION AA, AB, AC, AD & AE

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-8116 FAX: (408) 482-8874 TWS: 910-338-2070	
DECIMAL	±		
XX±			
XXX±			
APPROVALS	DATE	TITLE PS PACKAGE OUTLINE	
DRAWN <i>AA</i>	03/15/98	.300" BODY WIDTH SOIC	
CHECKED		.050" PITCH	
		SIZE C	DRAWING No. PSC-4007
			REV 06
DO NOT SCALE DRAWING			

4825771 0021977 67T

SSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
25338	00	INITIAL RELEASE	12/16/93	T. WJ
27495	01	REDRAW TO JEDEC FORMAT	03/10/95	T. WJ
28047	02	ADD 28 LD	08/15/95	



TOLERANCES UNLESS SPECIFIED			Integrated Device Technology, Inc.	
DECIMAL	ANGULAR		2975 Stender Way, Santa Clara, CA 95054	
DIGIT	°		PHONE: (408) 727-6118	
POOR	'		FAX: (408) 482-8874 TDD: 910-338-2070	
CHECKS:				
APPROVALS	DATE	TITLE		
DRAWN <i>Ad</i>	12/15/93	PC PACKAGE OUTLINE		
CHECKED		.150" BODY WIDTH SSOP		
		.025" PITCH		
		SIZE C	DRAWING No.	REV
			PSC - 4040	02
DO NOT SCALE DRAWING				

PACKAGE DIAGRAM OUTLINES

SSOP (Continued)

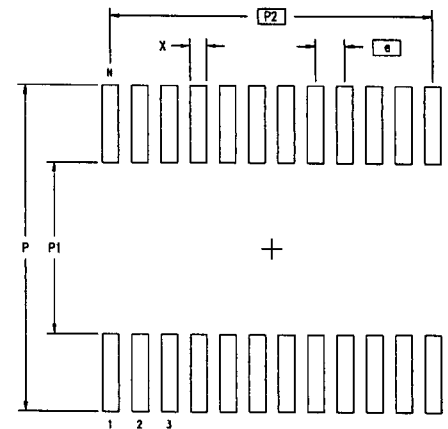
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	JEDEC VARIATION			AB		JEDEC VARIATION			AD		JEDEC VARIATION			AE		JEDEC VARIATION			AF	
	MIN	NOM	MAX	MIN		NOM	MAX	MIN	NOM		MAX	MIN	NOM	MAX		MIN	NOM	MAX		
A	.061	.064	.068			.061	.064	.068			.061	.064	.068			.061	.064	.068		
A1	.004	.006	.010			.004	.006	.010			.004	.006	.010			.004	.006	.010		
A2	.055	.058	.061	11		.055	.058	.061	11		.055	.058	.061	11		.055	.058	.061	11	
D	.189	.194	.196	4,5		.337	.342	.344	4,5		.337	.342	.344	4,5		.386	.390	.394	4,5	
E	.230	.236	.244	3		.230	.236	.244	3		.230	.236	.244	3		.230	.236	.244	3	
E1	.150	.155	.157	4,6		.150	.155	.157	4,6		.150	.155	.157	4,6		.150	.155	.157	4,6	
N		16					20					24					28			

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS $\square$ -A- AND $\square$ -B- TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION E TO BE DETERMINED AT SEATING PLANE $\square$ -C-
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
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- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-137, VARIATION AB, AD, AE & AF. EXCEPTIONS: JEDEC DIMENSION A2 MAX IS .059

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
25338	00	INITIAL RELEASE	12/16/93	T. VU
27495	01	REDRAW TO JEDEC FORMAT	03/10/95	T. VU
28047	02	ADD 28 LD	08/15/95	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	.274	.282	.274	.282	.274	.282	.274	.282
P1	.142	.150	.142	.150	.142	.150	.142	.150
P2	.175 BSC		.225 BSC		.275 BSC		.325 BSC	
X	.010	.018	.010	.018	.010	.018	.010	.018
e	.025 BSC		.025 BSC		.025 BSC		.025 BSC	
N	16		20		24		28	

TOLERANCES UNLESS SPECIFIED		INTEGRATED DEVICE TECHNOLOGY, INC. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 482-8874 TWR: 910-338-2070
DECIMAL	ANGULAR	
±	±	
XXX±	XXX±	
XXXX±	XXXX±	
APPROVALS	DATE	TITLE
DRAWN	12/15/93	PC PACKAGE OUTLINE
CHECKED		.150" BODY WIDTH SSOP
		.025" PITCH
		SIZE C DRAWING No. PSC-4040
		DO NOT SCALE DRAWING
		REV 02

4825771 0021986 682

117