T-49-11-00

National Semiconductor

DM74AS881B 4-Bit Arithmetic Logic Unit/Function Generator

General Description

The DM74AS881B is an arithmetic logic unit (ALU)/function generator that has a complexity of 77 equivalent gates, respectively, on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables I and II. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the DM74AS882 full carry look-ahead circuits, high speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multi-level full carry look-ahead is illustrated under "signal designations."

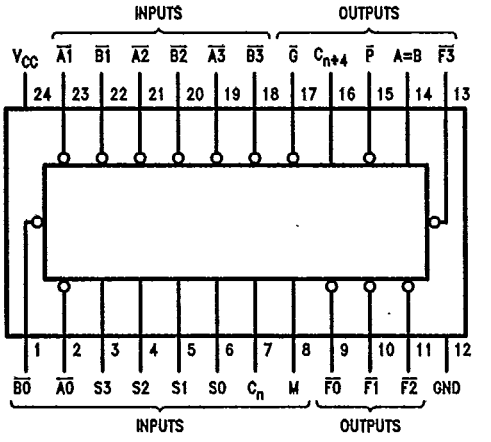
If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word-lengths can be performed without external circuitry.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky TTL counterpart
- Improved AC performance over Schottky counterpart
- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high speed operations on long words

Connection Diagram

Dual-In-Line Package



TL/F/6336-1

Top View

Order Number DM74AS881BNT
See NS Package Number N24C*

Pin Designations

Designation	Pin Number	Function
$\overline{A3}$, $\overline{A2}$, $\overline{A1}$, $\overline{A0}$	19, 21, 23, 2	Word A Inputs
$\overline{B3}$, $\overline{B2}$, $\overline{B1}$, $\overline{B0}$	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
$\overline{F3}$, $\overline{F2}$, $\overline{F1}$, $\overline{F0}$	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
$\overline{P}$	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
$\overline{G}$	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

*Contact your local NSC representative about surface mount (M) package availability.

T-49-11

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA} N Package	48.5°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{OH}	High Level Output Voltage A = B Output Only				5.5	V
I_{OH}	High Level Output Current	All Outputs Except A = B and $\overline{G}$			−2	mA
		$\overline{G}$			−3	
I_{OL}	Low Level Output Current	All Outputs Except $\overline{G}$			20	mA
		$\overline{G}$			48	
T_A	Operating Free Air Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA	Any Output Except A = B	V_{CC} − 2			V
		V_{CC} = 4.5V, I_{OH} = −3 mA	$\overline{G}$	2.4	3.4		
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V	A = B			0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA	Any Output Except $\overline{G}$		0.3	0.5	V
		V_{CC} = 4.5V, I_{OL} = 48 mA	$\overline{G}$		0.4	0.5	
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_I = 7V	M Input			0.1	mA
			Any $\overline{A}$ or $\overline{B}$ Input			0.3	
			Any S Input			0.4	
			Carry Input			0.6	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V	M Input			20	µA
			Any $\overline{A}$ or $\overline{B}$ Input			60	
			Any S Input			80	
			Carry Input			120	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V	M Input			−0.5	mA
			Any $\overline{A}$ or $\overline{B}$ Input			−1.5	
			Any S Input			−2	
			Carry Input			−3	
I_O (Note 2)	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	All Outputs Except A = B and $\overline{G}$	−30		−112	mA
			$\overline{G}$		−165		
I_{CC}	Supply Current	V_{CC} = 5.5V			70	104	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

T-49-11

Switching Characteristics

Symbol	Parameter	Conditions	From (Input)	To (Output)	C_L = 50 pF (15 pF for A = B), R_L = 500Ω (280Ω for A = B)		Units
					Min	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		C_n	C_{n+4}	2	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	12	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ Mode)	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	2	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	2	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	19	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V ($\overline{SUM}$ or $\overline{DIFF}$ Mode)	C_n	Any $\overline{F}$	3	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				3	12	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ Mode)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	2	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	10	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	2	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	12	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ Mode)	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	2	11	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	11	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	2	13	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	13	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ Mode)	$\overline{A_i}$ or $\overline{B_i}$	$\overline{F_i}$	2	11	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	11	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	$\overline{A_i}$ or $\overline{B_i}$	$\overline{F_i}$	2	13	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	13	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 4.5V (Logic Mode)	$\overline{A_i}$ or $\overline{B_i}$	$\overline{F_i}$	2	14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	14	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	Any $\overline{A}$ or $\overline{B}$	A = B	4	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				4	24	

Switching Characteristics (Continued)

T-49-11

Symbol	Parameter	Conditions	From (Input)	To (Output)	C_L = 50 pF (15 pF for A = B), R_L = 500Ω (280Ω for A = B)		Units
					Min	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n = M = S0 = S3 = 4.5V, S1 = S2 = 0V, Equality ($A_i = B_i$ or $A_i \neq B_i$)	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	2	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	18	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n = M = S3 = 4.5V, S1 = S2 = 0V, Equality ($A_i = B_i$ or $A_i \neq B_i$)	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	2	21	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	21	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n = m = S2 = 4.5V, S0 = S1 = S3 = 0V, ($A_i = B_i$ = H or A_i or B_i = L)	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	2	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	18	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n = M = S2 = 4.5V, S0 = S1 = S3 = 0V, ($A_i = B_i$ = H or A_i or B_i = L)	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	2	22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	22	

Number of Bits	Typical Addition Times Using AS881 and AS882	Package Count		Carry Method Between ALUs
		Arithmetic/ Logic Units	Look-Ahead Carry Generators	
1 to 4	5	1	0	None
5 to 8	10	2	0	Ripple
9 to 16	14	3 or 4	1	Full Look-Ahead
17 to 64	19	5 to 16	2 to 5	Full Look-Ahead

Functional Description

The DM74AS881B will accommodate active-high or active-low data if the pin designations are interpreted as follows:

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low Data (Table I)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-High Data (Table II)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A − B − 1, which requires an end-around or forced carry to provide A − B.

The DM74AS881B can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function-select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

Input C_n	Output C_{n+4}	Active-Low Data *(Figure 1)*	Active-High Data *(Figure 2)*
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables I and II and include exclusive-OR, NAND, AND, NOR, and OR functions.

T-49-11

881B

Functional Description (Continued)

TABLE I

Selection				Active-Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (No Carry)	C_n = H (With Carry)
L	L	L	L	$F = \overline{A}$	F = A Minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = $A\overline{B}$ Minus 1	F = $A\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Comp)	F = Zero
L	H	L	L	$F = \overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	$F = \overline{B}$	F = AB Plus (A + $\overline{B}$)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A + \overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	$F = \overline{A}B$	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	$F = A \oplus B$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = $A\overline{B}$ Plus (A + B)	F = $A\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = $A\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = $A\overline{B}$ Plus A	F = $A\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

TABLE II

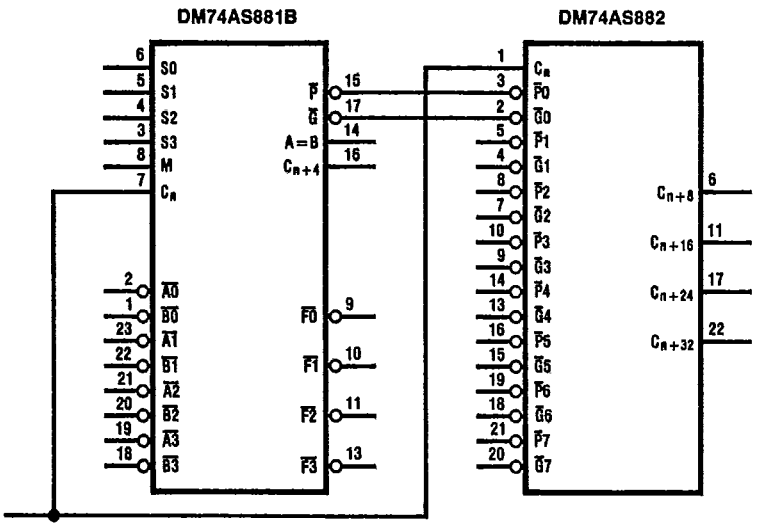
Selection				Active-High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	$\overline{C}_n$ = H (No Carry)	$\overline{C}_n$ = L (With Carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A Plus 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Comp)	F = Zero
L	H	L	L	F = $\overline{AB}$	F = A Plus $A\overline{B}$	F = A Plus $A\overline{B}$ Plus 1
L	H	L	H	$F = \overline{B}$	F = (A + $\overline{B}$) Plus $A\overline{B}$	F = (A + B) Plus $A\overline{B}$ Plus 1
L	H	H	L	$F = A \oplus B$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = $A\overline{B}$	F = $A\overline{B}$ Minus 1	F = $A\overline{B}$
H	L	L	L	F = $\overline{A} + B$	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.

3

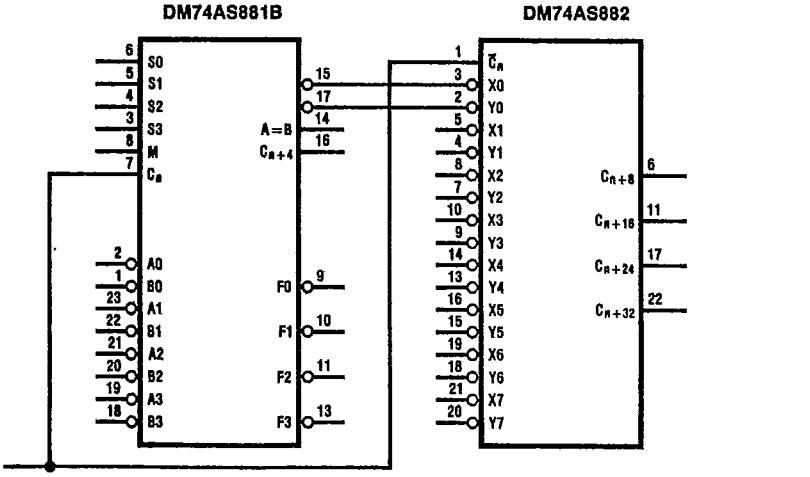
T-49-11

Functional Description (Continued)



TL/F/6336–2

FIGURE 1 (Use with Table I)



TL/F/6336–3

FIGURE 2 (Use with Table II)

T-49-11

Functional Description (Continued)

The DM74AS881B has the same pinout and same functionality as the DM74AS181B, except for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M = H).

In the logic mode, the DM74AS881B provides the user with a status check on the input words, A and B, and the output word, F. While in the logic mode, the $\overline{P}$, $\overline{G}$ and C_{n+4} outputs supply status information based upon the following logical combinations:

$$\overline{P} = F0 + F1 + F2 + F3$$

$$\overline{G} = H$$

$$C_{n+4} = PC_n.$$

The combination of signals on the S3 through S0 control lines determines the operation performed on the data words to generate the output bits, F_i. By monitoring the $\overline{P}$ and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see Function Table for Input Bits Equal/Not Equal) or if any pair of inputs is high (see Function Table for Input Pairs High/Not High). The DM74AS881B has the unique feature of providing an A = B status while the exclusive-OR ($\oplus$) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H, a status check is generated to determine whether all pairs (A_i, B_i) are equal in the following manner: $\overline{P} = (A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3)$. This unique bit-by-bit comparison of the data words, which is available on the totem pole $\overline{P}$ output, is particularly useful when cascading in the DM74AS881B. As the A = B condition is sensed in the first stage, the signal is propagated through the same ports used for carry generation in the arithmetic mode ($\overline{P}$ and $\overline{G}$). Thus, the A = B status is transmitted to the second state more quickly without the need for external multiplexing logic. The A = B open-collector output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs ($\overline{A}_i$, $\overline{B}_i$) being high, it is necessary to set the control lines (S3, S2, S1, S0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\overline{P} = \overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$.

S3	S2	S1	S0	M	$\overline{P}$ = F0 + F1 + F2 + F3
L	H	L	L	H	$\overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$
H	L	L	H	H	(A0 $\oplus$ B0) + (A1 $\oplus$ B1) + (A2 $\oplus$ B2) + (A3 $\oplus$ B3)

SIGNAL DESIGNATIONS

In both *Figures 1* and *2*, the polarity indicators indicate that the associated input or output is active-low with respect to the function shown inside the symbol, and that the symbols are the same in both figures. The signal designations in *Figure 1* agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table I. The signal designations have been changed in *Figure 2* to accommodate the logic functions and arithmetic operations for the active-high data given in Table II. The DM74AS181 and DM74AS881B, together with the DM74AS882 and DM74S182, can be used with the signal designation of either *Figure 1* or *Figure 2*.

Function Table for Input Pairs High/Not High
S0 = S1 = S3 = L, S2 = H, and M = H

C_n	Data Inputs				Outputs		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	A0 = B0	A1 = B1	A2 = B2	A3 = B3	H	L	H
L	A0 = B0	A1 = B1	A2 = B2	A3 = B3	H	L	L
X	A0 $\neq$ B0	X	X	X	H	H	L
X	X	A1 $\neq$ B1	X	X	H	H	L
X	X	X	A2 $\neq$ B2	X	H	H	L
X	X	X	X	A3 $\neq$ B3	H	H	L

Function Table for Input Bits Equal/Not Equal
S0 = S3 = H, S1 = S2 = L, and M = H

C_n	Data Inputs				Outputs		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	H
L	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	L
X	$\overline{A}0 = \overline{B}0$ = H	X	X	X	H	H	L
X	X	$\overline{A}1 = \overline{B}1$ = H	X	X	H	H	L
X	X	X	$\overline{A}2 = \overline{B}2$ = H	X	H	H	L
X	X	X	X	$\overline{A}3 = \overline{B}3$ = H	H	H	L

T-49-11

Parameter Measurement Information

$\overline{SUM}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$C_n + 4$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

T-49-11

Parameter Measurement Information (Continued)

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

$\overline{\text{DIFF}}$ Mode Test Table
Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

T-49-11

Parameter Measurement Information (Continued)

$\overline{\text{DIFF}}$ Mode Test Table (Continued)
Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	Remaining or Any $\overline{F}$	A = B	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or Any $\overline{F}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	NONE	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

Input Bits Equal/Not Equal Test Table
Function Inputs: S0 = S3 = M = 4.5V, S1 = S2 = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

Parameter Measurement Information (Continued)

T-49-11

Input Bits Equal/Not Equal Test Table (Continued)
Function Inputs: S0 = S3 = M = 4.5V, S1 = S2 = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

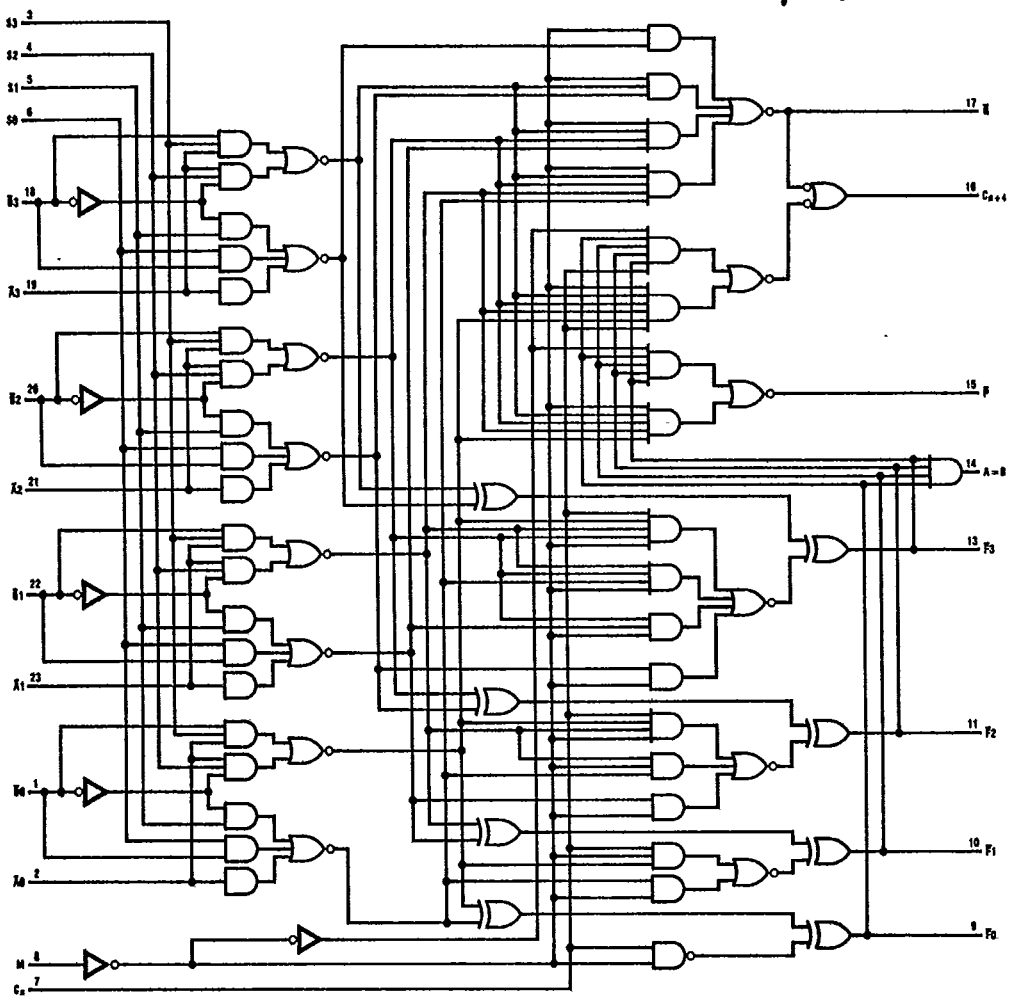
Input Pairs High/Not High Test Table
Function Inputs: S2 = M = 4.5V, S0 = S1 = S3 = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

Logic Diagram (Positive Logic)

T-49-11

74AS881B



TL/F/6336–4