



MC5480 • MC7480 MC9380 • MC8380

Add Suffix F for TO-86 ceramic package (Case 607)
 Suffix L for TO-116 ceramic package (Case 632)
 Suffix P for TO-116 plastic package (Case 646) MC7480, MC8380.

These devices are one-bit binary full adders with gated complementary inputs, complementary Sum and \bar{S} outputs, and an inverted Carry output. The circuit uses DTL inputs and a high-speed, high-fan-out, TTL "totem pole" configuration for the Sum, \bar{S} , and Carry outputs. The design of the high-speed carry circuitry reduces the need for external "look ahead carry" cascading in system designs. The use of low-level, low-power gates in a monolithic design provides significantly lower power dissipation than equivalent adders built from standard integrated circuits.

This full adder provides a basic building block for medium and high-speed, multiple-bit, parallel-add/serial-carry subsystems.

2

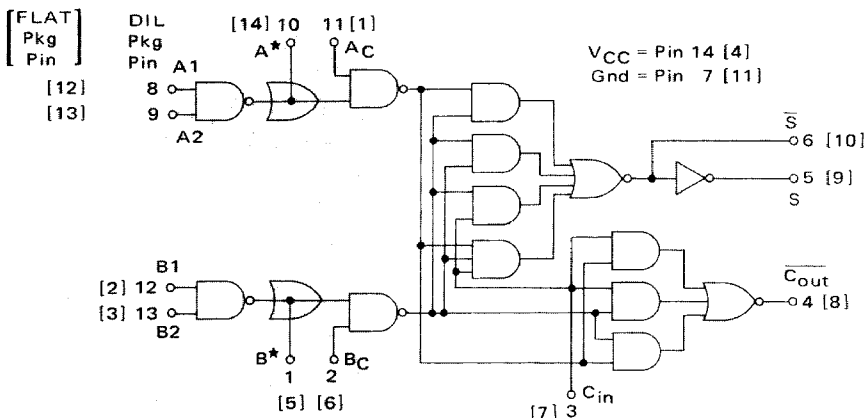
004477

4477

not

TRUTH TABLE

C _{in}	B	A	\bar{C}_{out}	\bar{S}	S
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1



1. $A = \overline{A^* \cdot A_C}$, $B = \overline{B^* \cdot B_C}$

where $A^* = \overline{A_1 \cdot A_2}$

$B^* = \overline{B_1 \cdot B_2}$

- When A^* (or B^*) is used as an input, A1 and A2 (or B1 and B2) must be connected to ground.
- When A1 and A2 (or B1 and B2) are used as inputs, A^* (or B^*) must be open, or used to perform wired-OR logic.

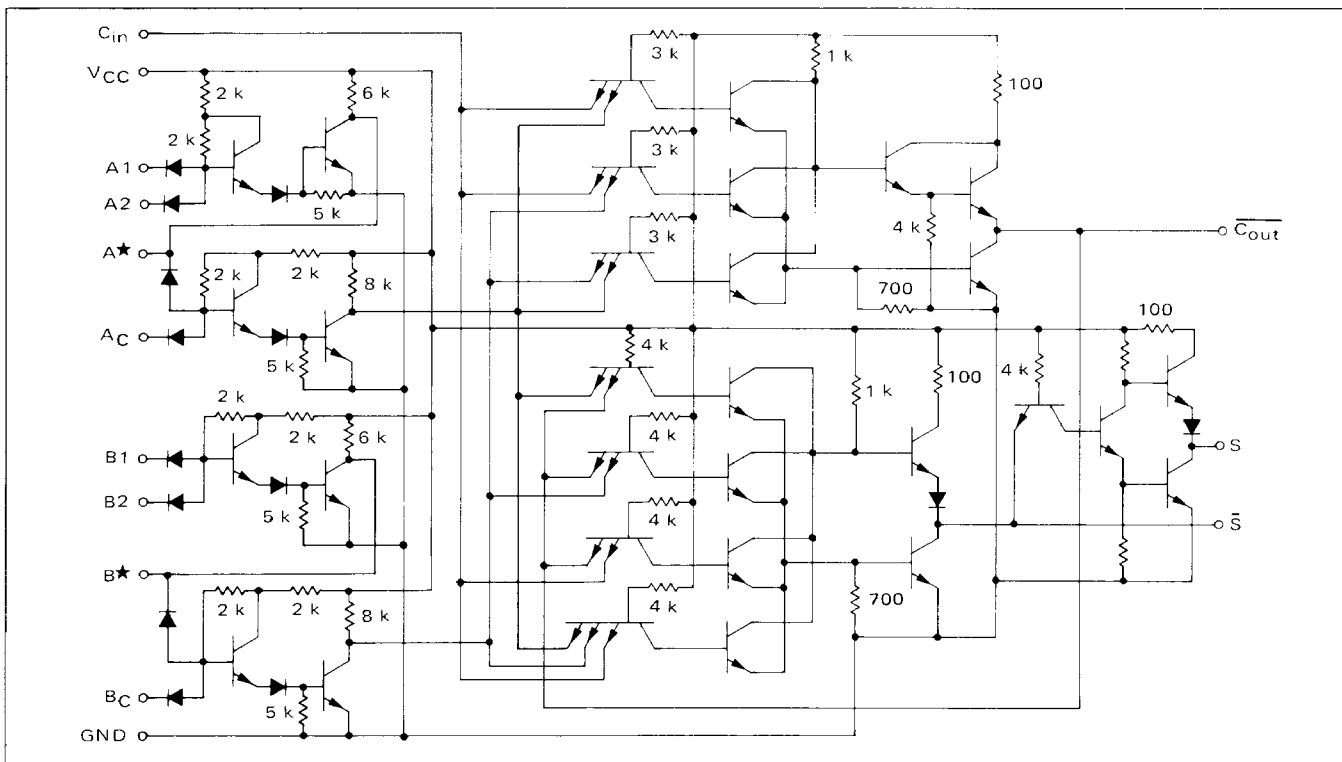
Input Loading Factor:

- A1, A2, A_C, B1, B2, B_C = 1
- A*, B* = 1.625
- C_{in} = 5

Output Loading Factor:

- \bar{C}_{out} = 5
- S, \bar{S} = 10
- A*, B* = 3

Total Power Dissipation = 105 mW typ/pkg



ELECTRICAL CHARACTERISTICS

Output voltage (logic level) tests are shown only for each output. The complete circuit can be tested by following the truth table.

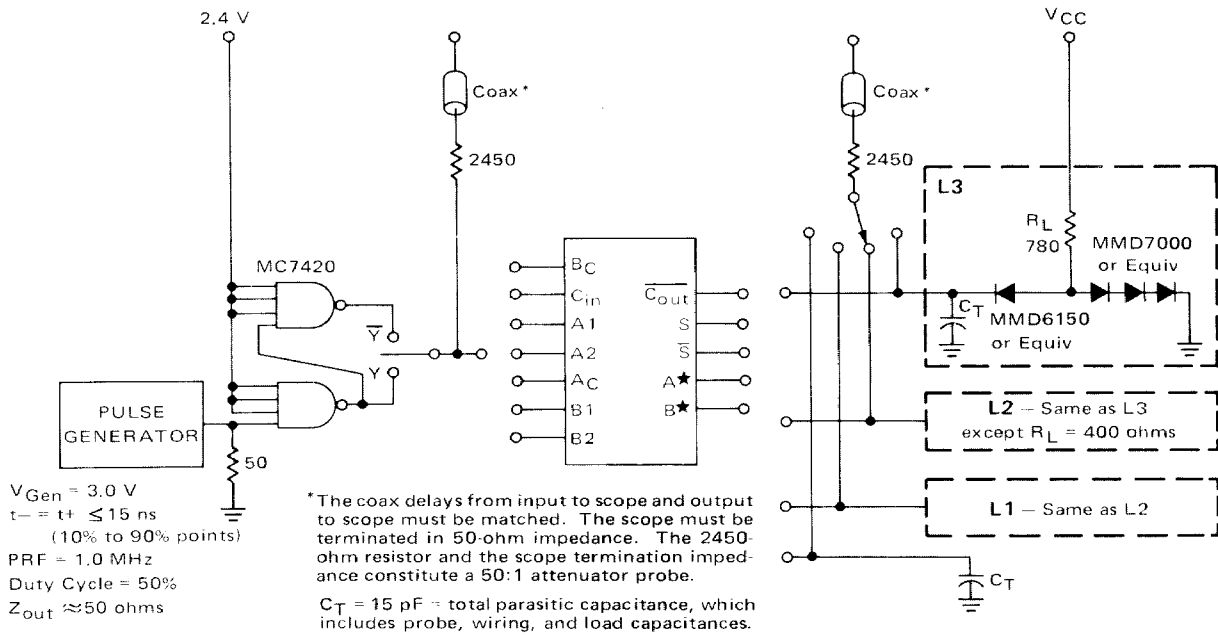
$V = V_{CC} = \text{Pin 14 [4]}$
 $\text{Gnd} = \text{Pin 7 [11]}$

Characteristic		Pin Under Test		TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
				mA						Volts					
				I _{OL1}	I _{OL2}	I _{OL3}	I _{OH1}	I _{OH2}	I _{OH3}	V _{IL}	V _{IH}	V _{ILT}	V _{IHT}	V _{CCL}	V _{CCH}
Input	Forward Current	MC5480, MC9380 Test Limits -55 to +125°C													
		MC7480, MC8380 Test Limits 0 to +75°C													
Input	Leakage Current	MC5480, MC9380 Test Limits -55 to +125°C													
		MC7480, MC8380 Test Limits 0 to +75°C													
Output	Output Voltage	MC5480, MC9380 Test Limits -55 to +125°C													
		MC7480, MC8380 Test Limits 0 to +75°C													
Output	Short-Circuit Current	MC5480, MC9380 Test Limits -55 to +125°C													
		MC7480, MC8380 Test Limits 0 to +75°C													
Power Requirements	Power Supply Drain	MC5480, MC9380 Test Limits -55 to +125°C													
		MC7480, MC8380 Test Limits 0 to +75°C													

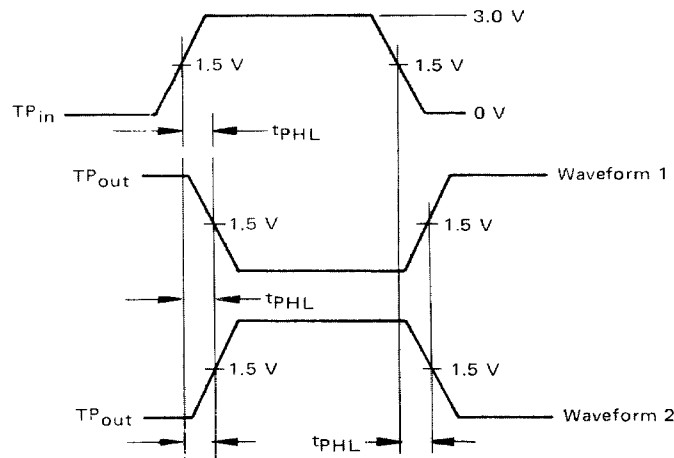
Pin 7 [11] is surrounded for all tests in addition to the pins listed below.

*Only one output should be shorted at a time.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



$V_{Gen} = 3.0 \text{ V}$
 $t_r = t_f \leq 15 \text{ ns}$
 (10% to 90% points)
 $PRF = 1.0 \text{ MHz}$
 Duty Cycle = 50%
 $Z_{out} \approx 50 \text{ ohms}$



TEST PROCEDURES ($T_A = 25^\circ\text{C}$)

TEST	PIN UNDER TEST	INPUT							OUTPUT					MAX LIMIT	WAVEFORM
		BC Pin 2 [6]	C _{in} Pin 3 [7]	A1 Pin 8 [12]	A2 Pin 9 [13]	A _c Pin 11 [1]	B1 Pin 12 [2]	B2 Pin 13 [3]	C _{out} Pin 4 [8]	S Pin 5 [9]	S Pin 6 [10]	A* Pin 10 [14]	B* Pin 1 [5]		
t _{PLH} C _{out}	4 [8]		Y				Gnd		L3					17 ns	1
t _{PHL} C _{out}			Y				Gnd		L3					12 ns	1
t _{PLH} C _{out}		Y	2.4 V	Gnd			Gnd		L3					25 ns	2
t _{PHL} C _{out}		Y	2.4 V	Gnd			Gnd		L3					55 ns	2
t _{PLH} S	5 [9]		2.4 V	Gnd		Y	Gnd		L3	L1	L2			70 ns	2
t _{PHL} S	5 [9]		2.4 V	Gnd		Y	Gnd		L3	L1	L2			80 ns	2
t _{PLH} S	6 [10]	Y	2.4 V				Gnd				L2			55 ns	2
t _{PHL} S	6 [10]	Y	2.4 V				Gnd				L2			75 ns	2
t _{PLH} A*	10 [14]			Y	2.4 V							C _T		65 ns	1
t _{PHL} A*	10 [14]			Y	2.4 V							C _T		25 ns	1
t _{PLH} B*	1 [5]					Y	2.4 V						C-	65 ns	1
t _{PHL} B*	1 [5]					Y	2.4 V						C-	25 ns	1