National Semiconductor

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LMV981 Single / LMV982 Dual

1.8V, RRIO Operational Amplifiers with Shutdown

General Description

LMV981/LMV982 are low voltage, low power operational amplifiers. LMV981/LMV982 operate from +1.8V to +5.0V supply voltages and have rail-to-rail input and output. LMV981/LMV982 input common mode voltage extends 200mV beyond the supplies which enables user enhanced functionality beyond the supply voltage range. The output can swing rail-to-rail unloaded and within 105mV from the rail with 600Ω load at 1.8V supply. LMV981/LMV982 are optimized to work at 1.8V which make them ideal for portable two-cell battery powered systems and single cell Li-Ion systems.

LMV981/LMV982 offer a shutdown pin that can be used to disable the device and reduce the supply current. The device is in shutdown when the $\overline{SHDN}$-pin = low. The output will be high impedance in shutdown.

LMV981/LMV982 exhibit excellent speed-power ratio, achieving 1.4MHz gain bandwidth product at 1.8V supply voltage with very low supply current. LMV981/LMV982 are capable of driving a 600Ω load and up to 1000pF capacitive load with minimal ringing. LMV981/LMV982 have a high DC gain of 101dB, making them suitable for low frequency applications.

LMV981 is offered in space saving 6-Bump micro SMD, SC70-6 and SOT23-6 packages. The 6-Bump micro SMD package has only a 1.006mm x 1.514mm x 0.945mm footprint. LMV982 is offered in space saving MSOP-10 package. These small packages are ideal solutions for area constrained PC boards and portable electronics such as cellular phones and PDAs.

Features

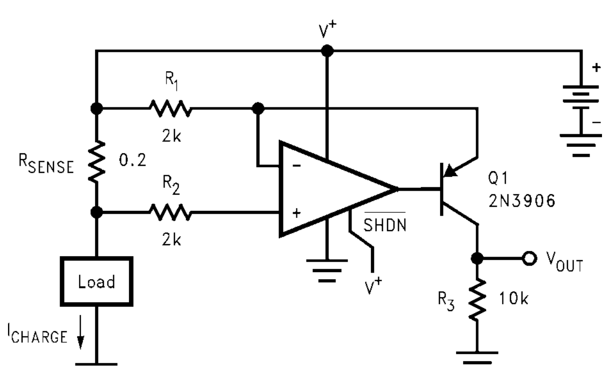
(Typical 1.8V Supply Values; Unless Otherwise Noted)

- Guaranteed 1.8V, 2.7V and 5V specifications
- Output swing
  - — w/600Ω load 80mV from rail
  - — w/2kΩ load 30mV from rail
- V_{CM} 200mV beyond rails
- Supply current (per channel) 100μA
- Gain bandwidth product 1.4MHz
- Maximum V_{OS} 4.0mV
- Gain w/600Ω load 101dB
- Ultra tiny package micro SMD 1.0mm x 1.5mm
- Turn-on time from shutdown 19μs
- Temperature range −40°C to 125°C

Applications

- Industrial and automotive
- Consumer communication
- Consumer computing
- PDAs
- Portable audio
- Portable/battery-powered electronic equipment
- Supply current monitoring
- Battery monitoring

Typical Application



$$V_{OUT} = \frac{R_{SENSE} \cdot R_3}{R_1} \cdot I_{Charge} = 1\Omega \cdot I_{Charge}$$

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	200V
Human Body Model	2000V
Supply Voltage ($V^+ – V^-$)	5.5V
Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pins	V^++0.3V, V^- -0.3V
Storage Temperature Range	−65°C to 150°C
Junction Temperature (Note 4)	150°C

For soldering specifications:

see product folder at www.national.com and www.national.com/ms/MS/MS-SOLDERING.pdf

Operating Ratings (Note 1)

Supply Voltage Range	1.8V to 5.0V
Temperature Range	−40°C to 125°C
Thermal Resistance (θ_{JA})	
6-Bump micro SMD	286°C/W
SC70-6	414°C/W
SOT23-6	265°C/W
MSOP-10	235°C/W

1.8V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (Note 10).

Symbol	Parameter	Condition		Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	LMV981 (Single)			1	4 **6**	mV
		LMV982 (Dual)			1	5.5 **7.5**	
TCV_{OS}	Input Offset Voltage Average Drift				5.5		μV/°C
I_B	Input Bias Current				15	35 **50**	nA
I_{OS}	Input Offset Current				13	25 **40**	nA
I_S	Supply Current (per channel)				103	185 **205**	μA
		In Shutdown	LMV981 (Single)		0.156	1 **2**	
			LMV982 (Dual)		0.178	3.5 **5**	
CMRR	Common Mode Rejection Ratio	LMV981, 0 ≤ V_{CM} ≤ 0.6V 1.4V ≤ V_{CM} ≤ 1.8V (Note 8)		60 **55**	78		dB
		LMV982, 0 ≤ V_{CM} ≤ 0.6V 1.4V ≤ V_{CM} ≤ 1.8V (Note 8)		55 **50**	76		
		−0.2V ≤ V_{CM} ≤ 0V 1.8V ≤ V_{CM} ≤ 2.0V		50	72		
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V		75 **70**	100		dB
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB	T_A = 25°C	V^- −0.2	−0.2 to 2.1	V^+ +0.2	V
			T_A = −40°C to 85°C	V^-		V^+	
			T_A = 125°C	V^- +0.2		V^+ −0.2	

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
A_V	Large Signal Voltage Gain LMV981 (Single)	$R_L = 600\Omega$ to 0.9V, $V_O = 0.2V$ to 1.6V, $V_{CM} = 0.5V$	77 **73**	101		dB
		$R_L = 2k\Omega$ to 0.9V, $V_O = 0.2V$ to 1.6V, $V_{CM} = 0.5V$	80 **75**	105		
	Large Signal Voltage Gain LMV982 (Dual)	$R_L = 600\Omega$ to 0.9V, $V_O = 0.2V$ to 1.6V, $V_{CM} = 0.5V$	75 **72**	90		dB
		$R_L = 2k\Omega$ to 0.9V, $V_O = 0.2V$ to 1.6V, $V_{CM} = 0.5V$	78 **75**	100		
V_O	Output Swing	$R_L = 600\Omega$ to 0.9V $V_{IN} = \pm 100mV$	1.65 **1.63**	1.72		V
				0.077	0.105 **0.120**	
		$R_L = 2k\Omega$ to 0.9V $V_{IN} = \pm 100mV$	1.75 **1.74**	1.77		
				0.024	0.035 **0.04**	
I_O	Output Short Circuit Current (Note 3)	Sourcing, $V_O = 0V$ $V_{IN} = 100mV$	4 **3.3**	8		mA
		Sinking, $V_O = 1.8V$ $V_{IN} = -100mV$	7 **5**	9		
Ton	Turn-on Time from Shutdown			19		µs
V_{SHDN}	Turn-on Voltage to enable part			1.0		V
	Turn-off Voltage			0.55		

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. $V^+ = 1.8V$, $V^- = 0V$, $V_{CM} = V^+/2$, $V_O = V^+/2$, $R_L > 1 M\Omega$ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (Note 10).

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	(Note 7)		0.35		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			67		deg
G_m	Gain Margin			7		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, $V_{CM} = 0.5V$		60		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1kHz, $A_V = +1$ $R_L = 600\Omega$, $V_{IN} = 1 V_{PP}$		0.023		%
	Amp-to-Amp Isolation	(Note 9)		123		dB

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V^+/2$, $V_O = V^+/2$, $R_L > 1 M\Omega$ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (Note 10).

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	LMV981 (Single)		1	4 **6**	mV
		LMV982 (Dual)		1	6 **7.5**	mV

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
TCV_{OS}	Input Offset Voltage Average Drift			5.5		μV/°C
I_B	Input Bias Current			15	35 **50**	nA
I_{OS}	Input Offset Current			8	25 **40**	nA
I_S	Supply Current (per channel)			105	190 **210**	μA
		In Shutdown, LMV981 (Single)		0.061	1 **2**	
		In Shutdown, LMV982 (Dual)		0.101	3.5 **5**	
CMRR	Common Mode Rejection Ratio	LMV981, $0 \le V_{CM} \le 1.5V$ $2.3V \le V_{CM} \le 2.7V$ (Note 8)	60 **55**	81		dB
		LMV982, $0 \le V_{CM} \le 1.5V$ $2.3V \le V_{CM} \le 2.7V$ (Note 8)	55 **50**	80		
		$-0.2V \le V_{CM} \le 0V$ $2.7V \le V_{CM} \le 2.9V$	50	74		
PSRR	Power Supply Rejection Ratio	$1.8V \le V^+ \le 5V$ $V_{CM} = 0.5V$	75 **70**	100		dB
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB, $T_A = 25°C$	V^- −0.2	−0.2 to 3.0	V^++0.2	V
		For CMRR Range ≥ 50dB, $T_A = -40°C$ to $85°C$	V^-		V^+	
		For CMRR Range ≥ 50dB, $T_A = 125°C$	V^- +0.2		V^+−0.2	
A_V	Large Signal Voltage Gain LMV981(Single)	$R_L = 600\Omega$ to 1.35V, $V_O = 0.2V$ to 2.5V	87 **86**	104		dB
		$R_L = 2k\Omega$ to 1.35V, $V_O = 0.2V$ to 2.5V	92 **91**	110		
	Large Signal Voltage Gain LMV982 (Dual)	$R_L = 600\Omega$ to 1.35V, $V_O = 0.2V$ to 2.5V	78 **75**	90		
		$R_L = 2k\Omega$ to 1.35V, $V_O = 0.2V$ to 2.5V	81 **78**	100		
V_O	Output Swing	$R_L = 600\Omega$ to 1.35V $V_{IN} = \pm 100mV$	2.55 **2.53**	2.62		V
				0.083	0.110 **0.130**	
		$R_L = 2k\Omega$ to 1.35V $V_{IN} = \pm 100mV$	2.65 **2.64**	2.675		
				0.025	0.04 **0.045**	
I_O	Output Short Circuit Current (Note 3)	Sourcing, $V_O = 0V$ $V_{IN} = 100mV$	20 **15**	30		mA
		Sinking, $V_O = 0V$ $V_{IN} = -100mV$	18 **12**	25		
Ton	Turn-on Time from Shutdown			12.5		μs
V_{SHDN}	Turn-on Voltage to enable part			1.9		V
	Turn-off Voltage			0.8		

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (Note 10).

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	(Note 7)		0.4		V/μs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			70		deg
G_m	Gain Margin			7.5		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 0.5V		57		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = 1V_{PP}		0.022		%
	Amp-to-Amp Isolation	(Note 9)		123		dB

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (Note 10).

Symbol	Parameter	Condition		Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	LMV981 (Single)			1	4 **6**	mV
		LMV982 (Dual)			1	5.5 **7.5**	
TCV_{OS}	Input Offset Voltage Average Drift				5.5		μV/°C
I_B	Input Bias Current				14	35 **50**	nA
I_{OS}	Input Offset Current				9	25 **40**	nA
I_S	Supply Current (per Channel)				116	210 **230**	μA
		In Shutdown	LMV981 (Single)		0.201	1 **2**	μA
			LMV982 (Dual)		0.302	3.5 **5**	
CMRR	Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 3.8V 4.6V ≤ V_{CM} ≤ 5.0V (Note 8)		60 **55**	86		dB
		−0.2V ≤ V_{CM} ≤ 0V 5.0V ≤ V_{CM} ≤ 5.2V		50	78		
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V V_{CM} = 0.5V		75 **70**	100		dB
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB	T_A = 25°C	V^- −0.2	−0.2 to 5.3	V^+ +0.2	V
			T_A = −40°C to 85°C	V^-		V^+	
			T_A = 125°C	V^- +0.3		V^+ −0.3	

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
A_V	Large Signal Voltage Gain (LMV981 Single)	R_L = 600Ω to 2.5V, V_O = 0.2V to 4.8V	88 **87**	102		dB
		R_L = 2kΩ to 2.5V, V_O = 0.2V to 4.8V	94 **93**	113		
	Large Signal Voltage Gain LMV982 (Dual)	R_L = 600Ω to 2.5V, V_O = 0.2V to 4.8V	81 **78**	90		dB
		R_L = 2kΩ to 2.5V, V_O = 0.2V to 4.8V	85 **82**	100		
V_O	Output Swing	R_L = 600Ω to 2.5V V_{IN} = ±100mV (Note 8)	4.855 **4.835**	4.890		V
				0.120	0.160 **0.180**	
		R_L = 2kΩ to 2.5V V_{IN} = ±100mV	4.945 **4.935**	4.967		
				0.037	0.065 **0.075**	
I_O	Output Short Circuit Current (Note 3)	LMV981, Sourcing, V_O = 0V V_{IN} = 100mV	80 **68**	100		mA
		Sinking, V_O = 5V V_{IN} = −100mV	58 **45**	65		
Ton	Turn-on Time from Shutdown			8.4		µs
V_{SHDN}	Turn-on Voltage to enable part			4.2		V
	Turn-off Voltage			0.8		

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = 2.5V, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (Note 10).

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	(Note 7)		0.42		V/µs
GBW	Gain-Bandwidth Product			1.5		MHz
Φ_m	Phase Margin			71		deg
G_m	Gain Margin			8		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 1V		50		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_O = 1V_{PP}		0.022		%
	Amp-to-Amp Isolation	(Note 9)		123		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}-T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.

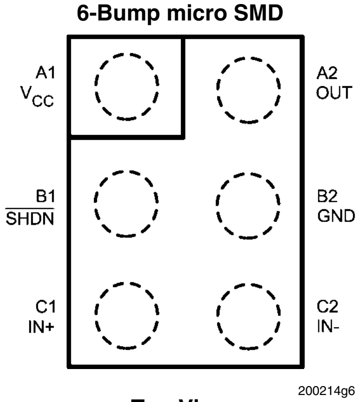
Note 8: For guaranteed temperature ranges, see Input Common-Mode Voltage Range specifications.

Note 9: Input referred, R_L = 100kΩ connected to $V^+/2$. Each amp excited in turn with 1kHz to produce $V_O = 3V_{PP}$. (For Supply Voltages <3V, $V_O = V^+$).

Note 10: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Applications section for information on temperature derating of this device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

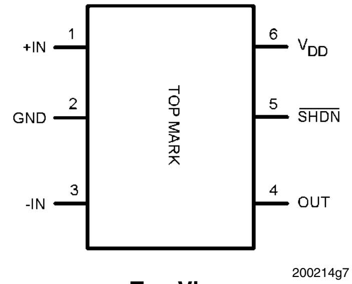
Connection Diagrams

6-Bump micro SMD



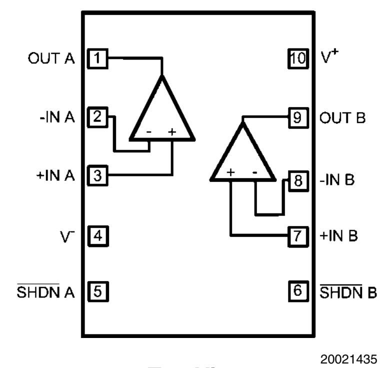
Top View

6-Pin SC70-6/SOT23-6



Top View

10-Pin MSOP



Top View

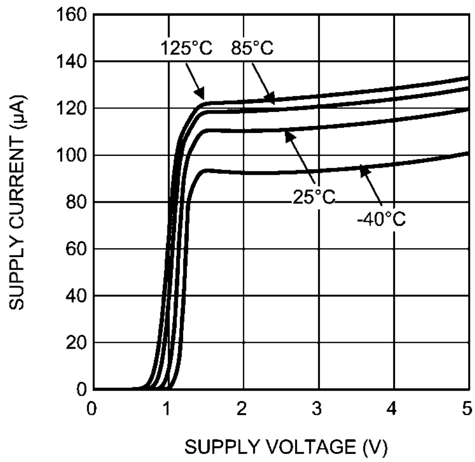
Ordering Information

Package	Part Number	Packaging Marking	Transport Media	NSC Drawing
6-Bump micro SMD (NOPB)	LMV981TL	H	250 Units Tape and Reel	TLA06BBA
	LMV981TLX		3k Units Tape and Reel	
6-Pin SC70	LMV981MG	A77	1k Units Tape and Reel	MA006A
	LMV981MGX		3k Units Tape and Reel	
6-Pin SOT23	LMV981MF	A78A	1k Units Tape and Reel	MF06A
	LMV981MFX		3.5k Units Tape and Reel	
10-Pin MSOP	LMV982MM	A87A	1k Units Tape and Reel	MUB10A
	LMV982MMX		3.5k Units Tape and Reel	

Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Supply Current vs. Supply Voltage (LMV981)



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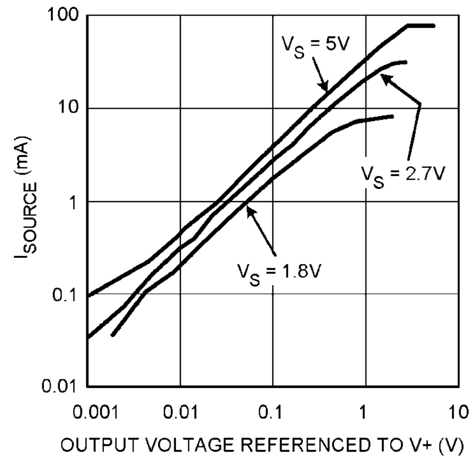
Sourcing Current vs. Output Voltage



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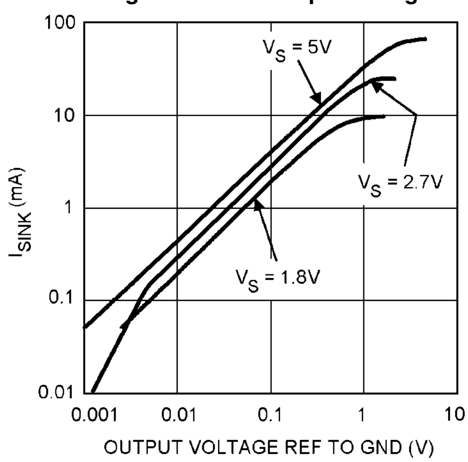
Sinking Current vs. Output Voltage



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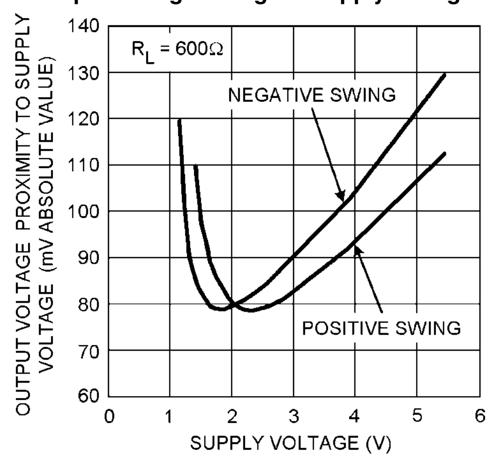
Output Voltage Swing vs. Supply Voltage



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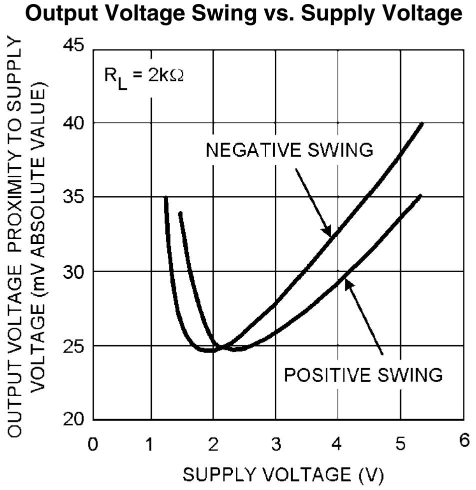
Output Voltage Swing vs. Supply Voltage



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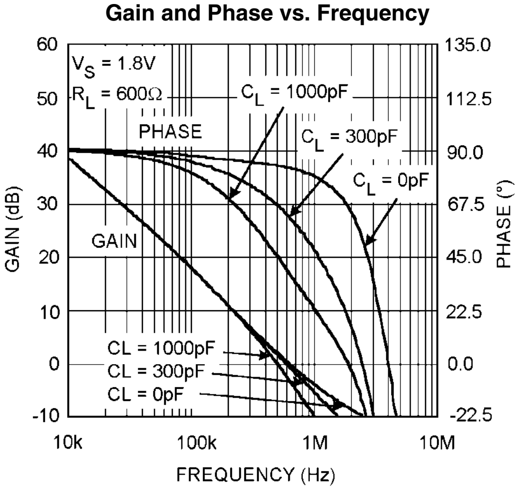
Gain and Phase vs. Frequency



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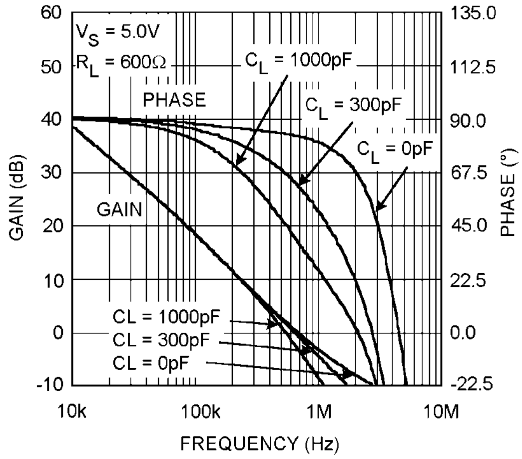
Gain and Phase vs. Frequency



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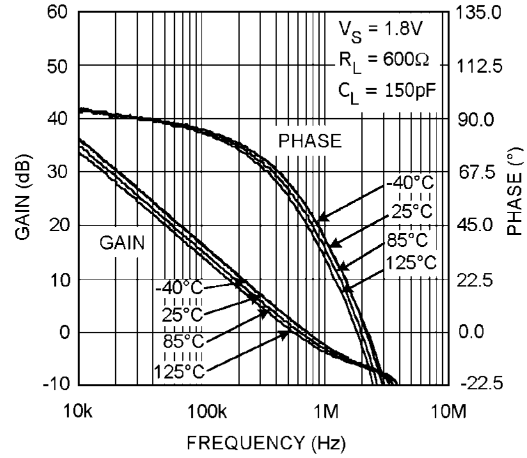
Gain and Phase vs. Frequency



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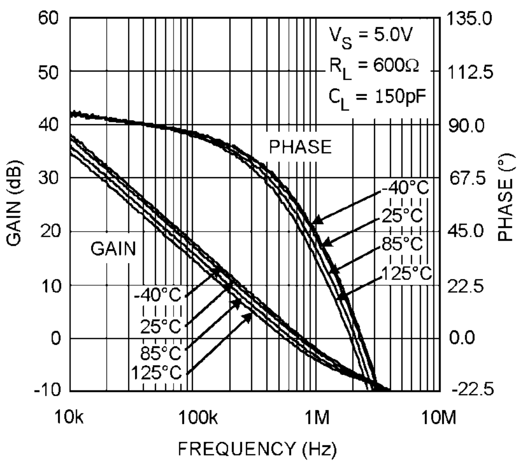
Gain and Phase vs. Frequency



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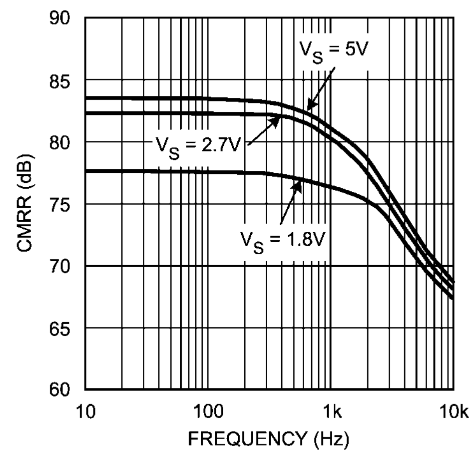
CMRR vs. Frequency



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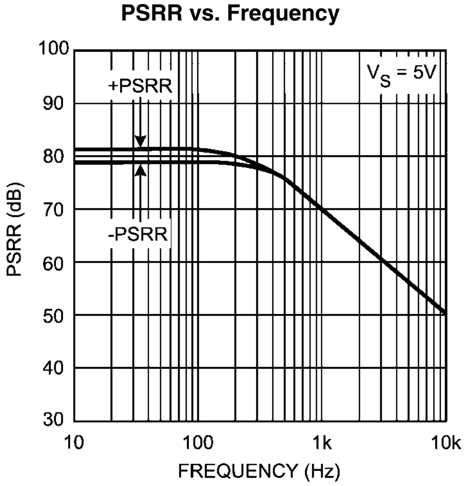
PSRR vs. Frequency



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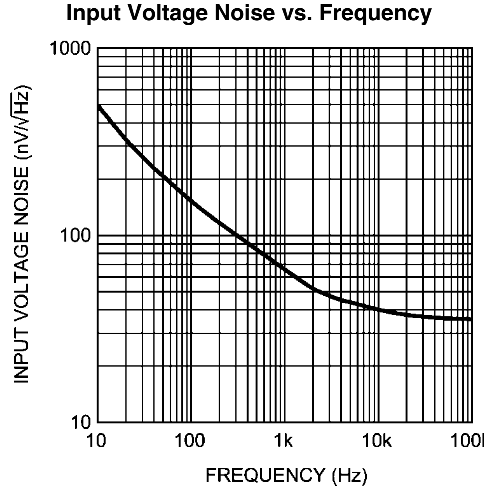
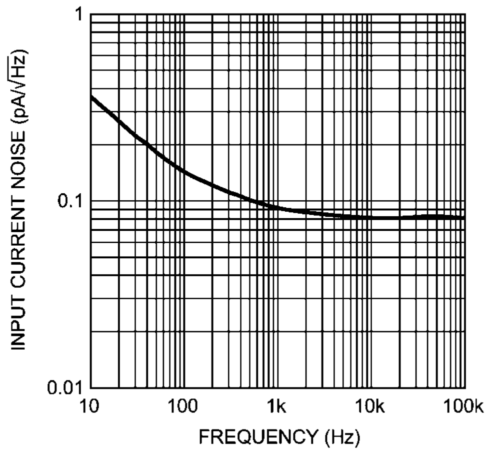
Input Voltage Noise vs. Frequency



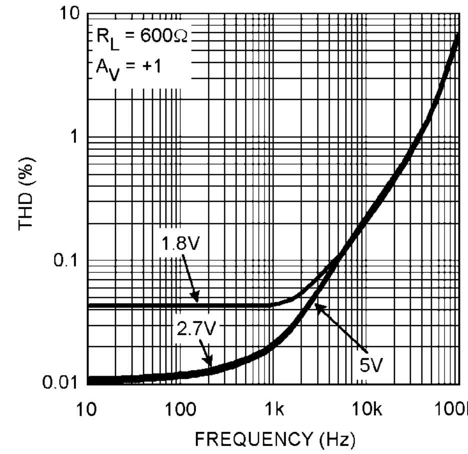
20021458

Input Current Noise vs. Frequency



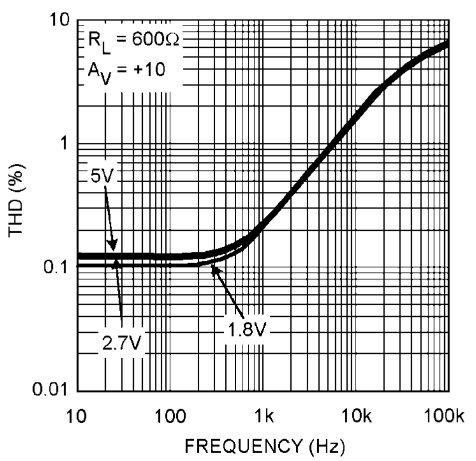
20021466

THD vs. Frequency



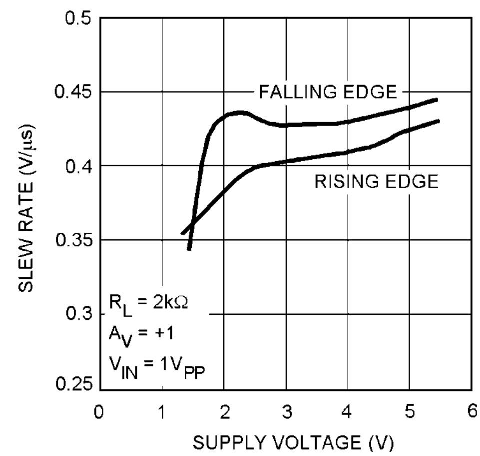
20021467

THD vs. Frequency



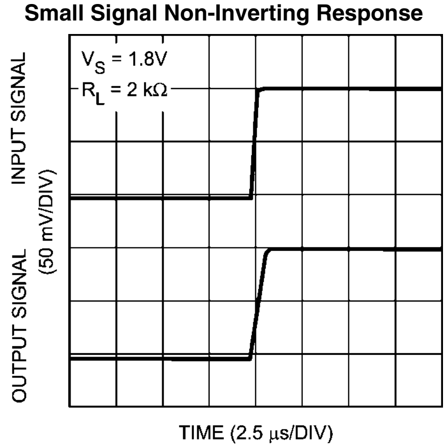
20021468

Slew Rate vs. Supply Voltage



20021469

Small Signal Non-Inverting Response



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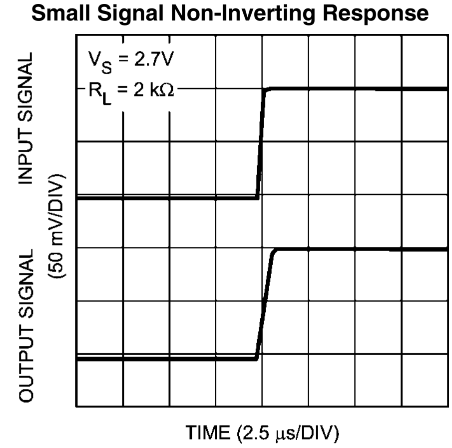
Small Signal Non-Inverting Response



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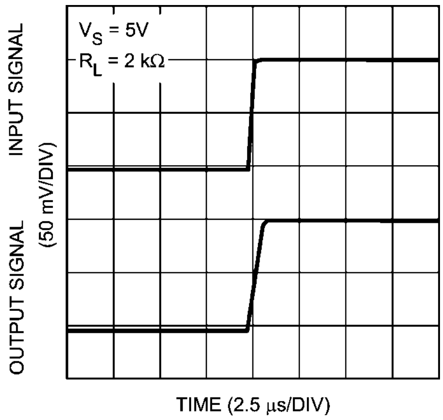

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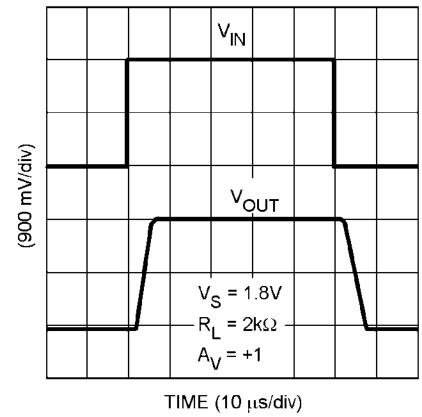

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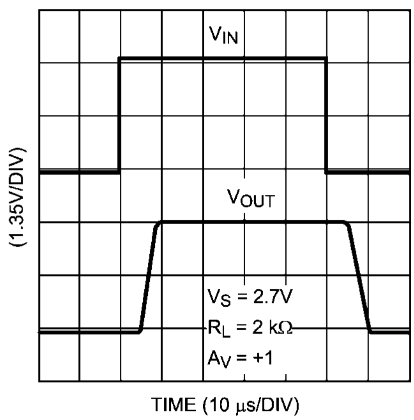
Large Signal Non-Inverting Response



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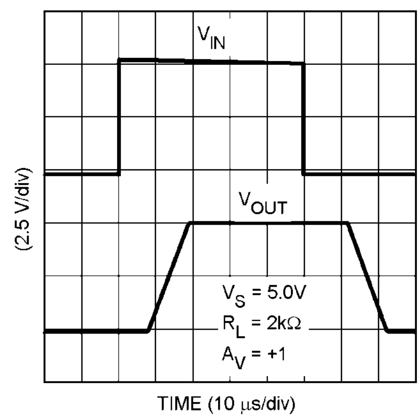
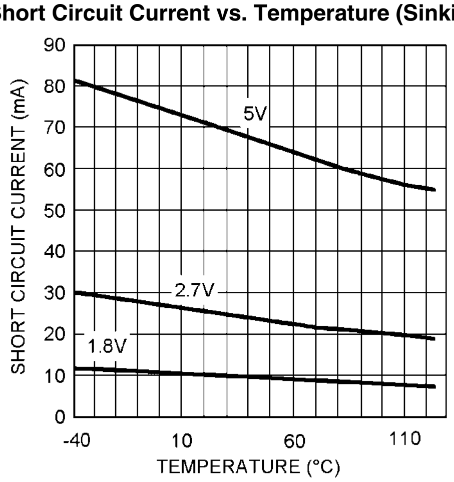
Large Signal Non-Inverting Response



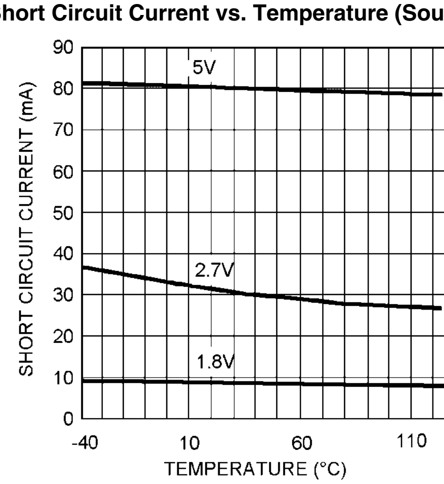
20021475

Short Circuit Current vs. Temperature (Sinking)



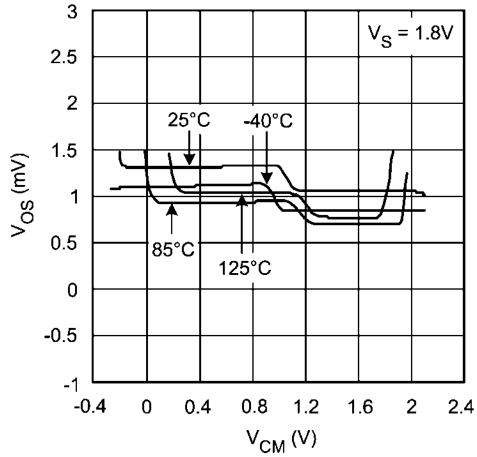
20021476

Short Circuit Current vs. Temperature (Sourcing)



20021477

Offset Voltage vs. Common Mode Range



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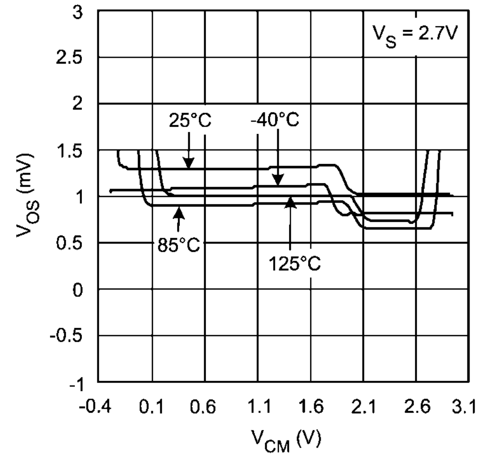
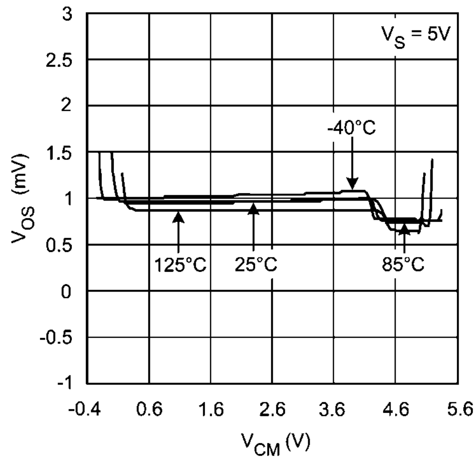
Offset Voltage vs. Common Mode Range



20021437

Offset Voltage vs. Common Mode Range



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Application Note

INPUT AND OUTPUT STAGE

The rail-to-rail input stage of this family provides more flexibility for the designer. The LMV981/LMV982 use a complimentary PNP and NPN input stage in which the PNP stage senses common mode voltage near V^- and the NPN stage senses common mode voltage near V^+. The transition from the PNP stage to NPN stage occurs 1V below V^+. Since both input stages have their own offset voltage, the offset of the amplifier becomes a function of the input common mode voltage and has a crossover point at 1V below V^+.

This V_{OS} crossover point can create problems for both DC and AC coupled signals if proper care is not taken. Large input signals that include the V_{OS} crossover point will cause distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover. For example, in a unity gain buffer configuration and with V_S = 5V, a 5V peak-to-peak signal will contain input-crossover distortion while a 3V peak-to-peak signal centered at 1.5V will not contain input-crossover distortion as it avoids the crossover point. Another way to avoid large signal distortion is to use a gain of –1 circuit which avoids any voltage excursions at the input terminals of the amplifier. In that circuit, the common mode DC voltage can be set at a level away from the V_{OS} cross-over point. For small signals, this transition in V_{OS} shows up as a V_{CM} dependent spurious signal in series with the input signal and can effectively degrade small signal parameters such as gain and common mode rejection ratio. To resolve this problem, the small signal should be placed such that it avoids the V_{OS} crossover point. In addition to the rail-to-rail performance, the output stage can provide enough output current to drive 600Ω loads. Because of the high current capability, care should be taken not to exceed the 150°C maximum junction temperature specification.

SHUTDOWN MODE

The LMV981/LMV982 have a shutdown pin. To conserve battery life in portable applications, the LMV981/LMV982 can be disabled when the shutdown pin voltage is pulled low.

The shutdown pin can't be left unconnected. In case shutdown operation is not needed, the shutdown pin should be connected to V^+ when the LMV981/LMV982 are used. Leaving the shutdown pin floating will result in an undefined operation mode, either shutdown or active, or even oscillating between the two modes.

INPUT BIAS CURRENT CONSIDERATION

The LMV981/LMV982 family has a complementary bipolar input stage. The typical input bias current (I_B) is 15nA. The input bias current can develop a significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 50nA and R_F is 100kΩ, then an offset voltage of 5mV will develop ($V_{OS} = I_B$ x R_F). Using a compensation resistor (R_C), as shown in *Figure 1*, cancels this effect. But the input offset current (I_{OS}) will still contribute to an offset voltage in the same manner.

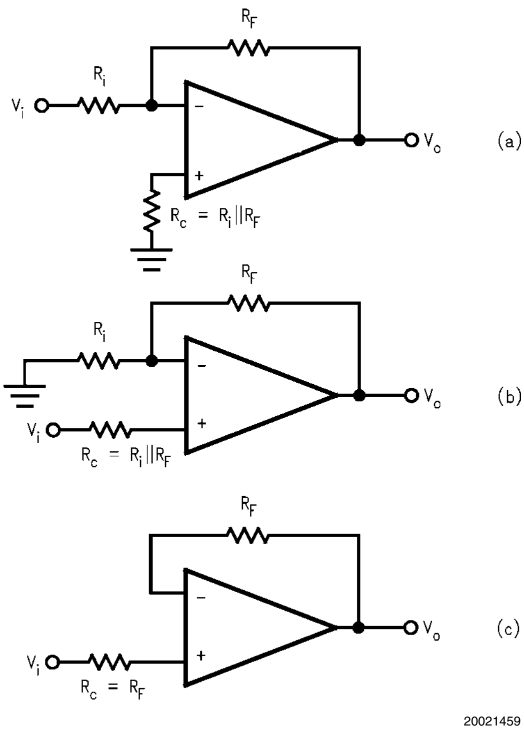
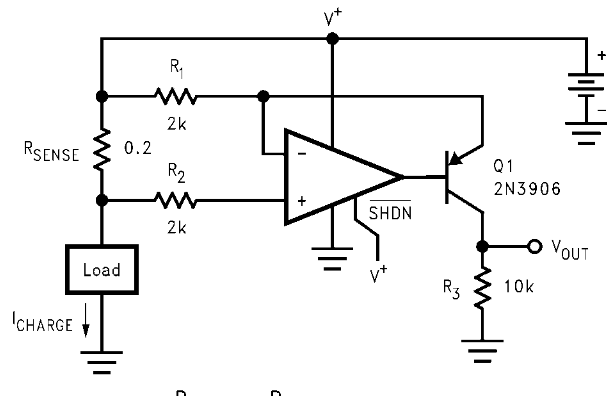


FIGURE 1. Canceling the Offset Voltage due to Input Bias Current

Typical Applications

HIGH SIDE CURRENT SENSING

The high side current sensing circuit (*Figure 2*) is commonly used in a battery charger to monitor charging current to prevent over charging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LMV981/LMV982 are ideal for this application because the common mode input range goes up to the rail.



$$V_{OUT} = \frac{R_{SENSE} \cdot R_3}{R_1} \cdot I_{Charge} = 1\,\Omega \cdot I_{Charge}$$

FIGURE 2. High Side Current Sensing

HALF-WAVE RECTIFIER WITH RAIL-TO-GROUND OUTPUT SWING

Since the LMV981/LMV982 input common mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction is an easy task. All that is needed are two external resistors; there is no need for diodes or matched resistors. The half wave rectifier can have either positive or negative going outputs, depending on the way the circuit is arranged.

In *Figure 3* the circuit is referenced to ground, while in *Figure 4* the circuit is biased to the positive supply. These configurations implement the half wave rectifier since the LMV981/LMV982 can not respond to one-half of the incoming waveform. It can not respond to one-half of the incoming because the amplifier can not swing the output beyond either rail therefore the output disengages during this half cycle. During the other half cycle, however, the amplifier achieves a half wave that can have a peak equal to the total supply voltage. R_I should be large enough not to load the LMV981/LMV982.

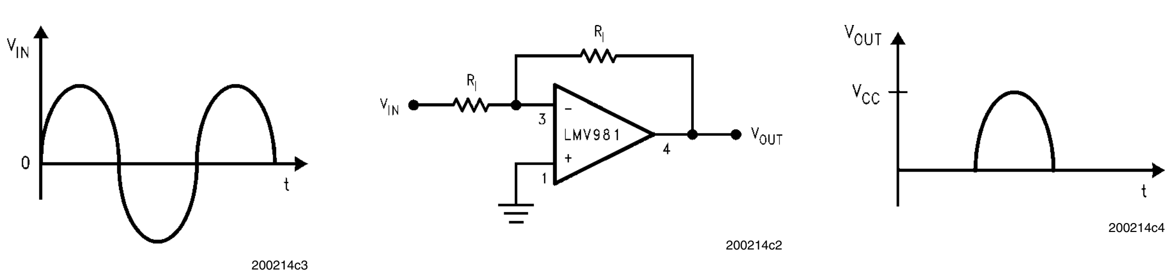


FIGURE 3. Half-Wave Rectifier with Rail-To-Ground Output Swing Referenced to Ground

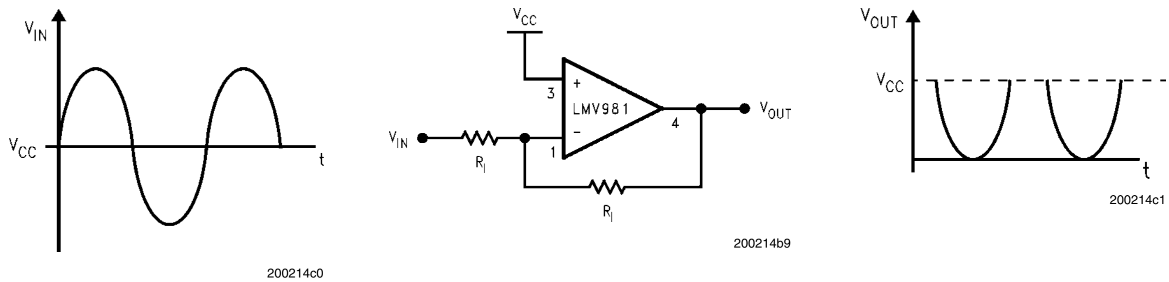


FIGURE 4. Half-Wave Rectifier with Negative-Going Output Referenced to V_{CC}

INSTRUMENTATION AMPLIFIER WITH RAIL-TO-RAIL INPUT AND OUTPUT

Some manufactures make a non-“rail-to-rail”-op amp rail-to-rail by using a resistive divider on the inputs. The resistors divide the input voltage to get a rail-to-rail input range. The problem with this method is that it also divides the signal, so in order to get the obtained gain, the amplifier must have a higher closed loop gain. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMRR as well. The LMV981/LMV982 is rail-to-rail and therefore doesn’t have these disadvantages.

Using three of the LMV981/LMV982 amplifiers, an instrumentation amplifier with rail-to-rail inputs and outputs can be made as shown in *Figure 5*.

In this example, amplifiers on the left side act as buffers to the differential stage. These buffers assure that the input impedance is very high and require no precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMRR set by the matching R_1-R_2 with R_3-R_4. The gain is set by the ratio of R_2/R_1 and R_3 should equal R_1 and R_4 equal R_2. With both rail-to-rail input and output ranges, the input and output are only limited by the supply voltages. Remember that even with rail-to-rail outputs, the output can not swing past the supplies so the combined common mode voltages plus the signal should not be greater that the supplies or limiting will occur. For additional applications, see National Semiconductor application notes AN–29, AN–31, AN–71, and AN–127.

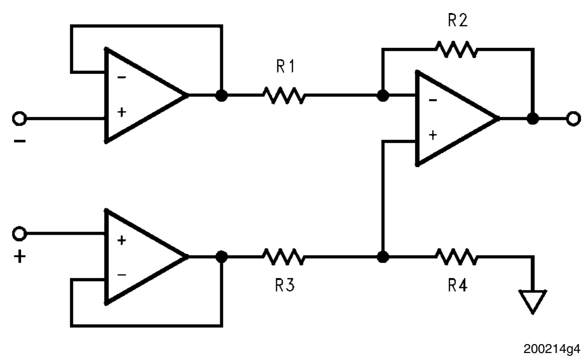
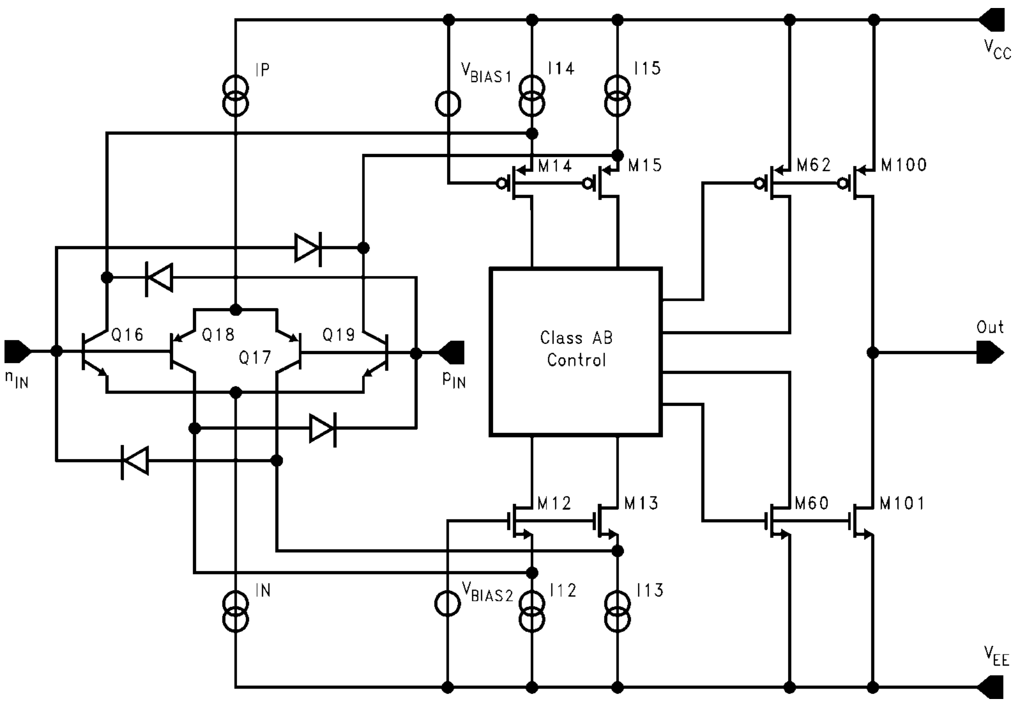


FIGURE 5. Rail-to-rail instrumentation amplifier

Simplified Schematic



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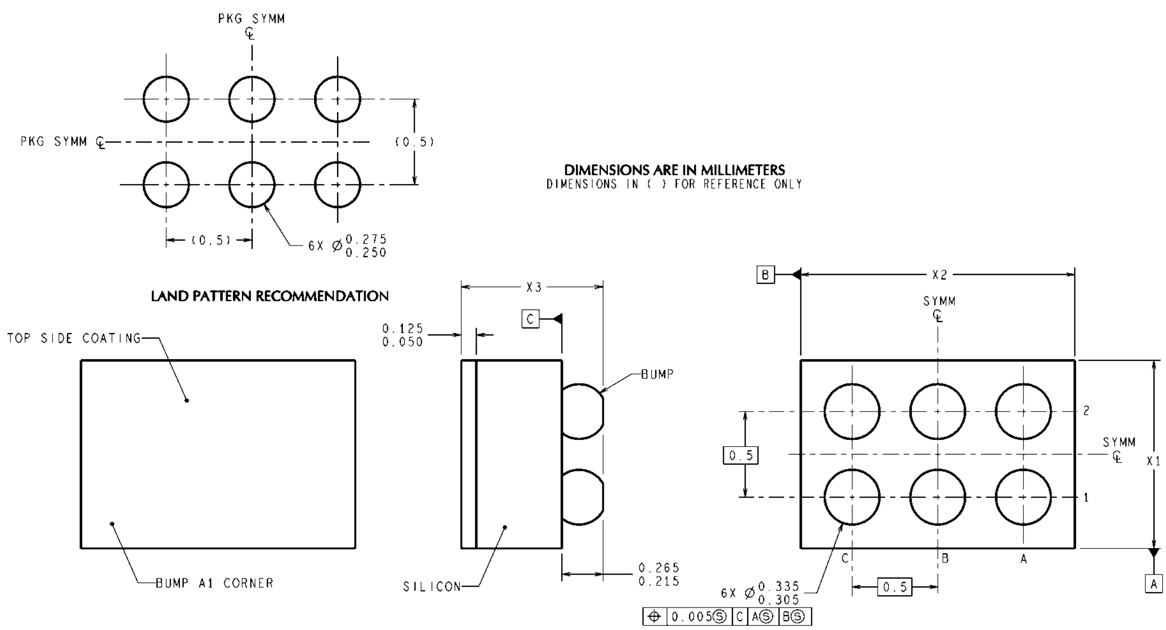
Physical Dimensions inches (millimeters) unless otherwise noted

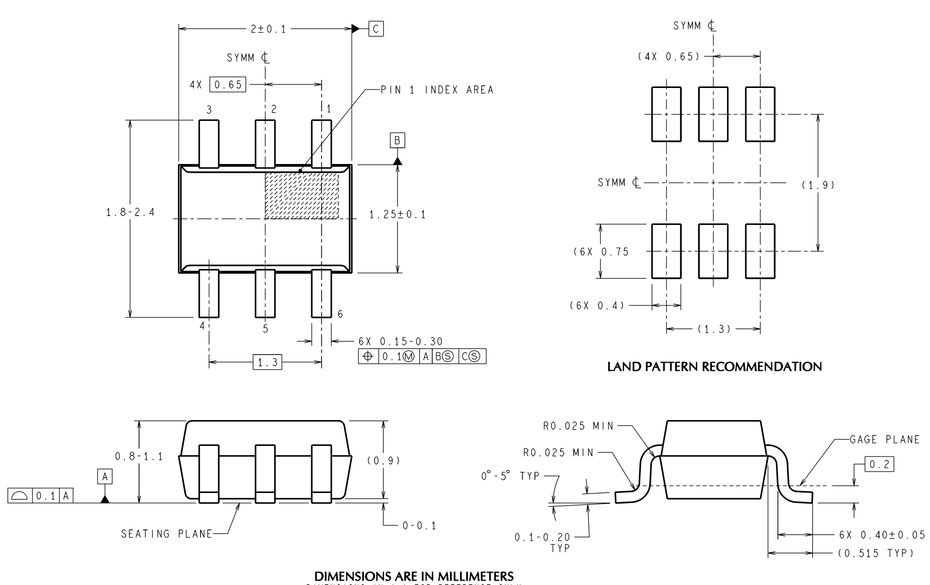


TLA06XXX (Rev C)

NOTES: UNLESS OTHERWISE SPECIFIED

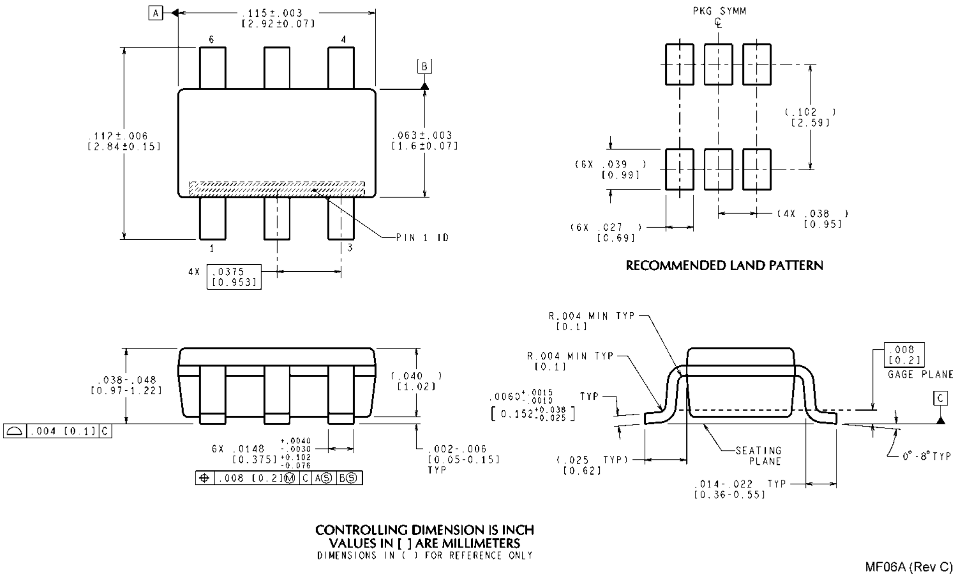
1. EPOXY COATING
2. FOR SOLDER BUMP COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATATION SEMICONDUCTOR WEB PAGE (www.national.com)
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN A1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION DB.

6-Bump micro SMD
NS Package Number TLA06BBA
X1 = 1.031 ±0.030mm X2 = 1.539 ±0.030mm X3 = 0.600 ±0.075mm

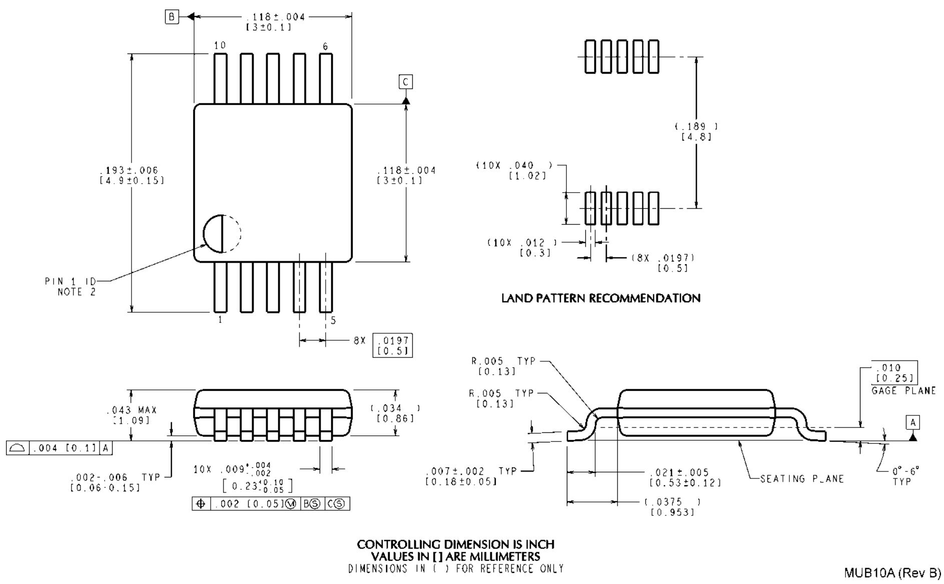


MAA06A (Rev B)

6-Pin SC70
NS Package Number MAA06A



6-Pin SOT23
NS Package Number MF06A



10-Pin MSOP
NS Package Number MUB10A

Notes

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