National Semiconductor

CLC034

OBSOLETE
September 21, 2011

SMPTE 292M / 259M Adaptive Cable Equalizer

General Description

The CLC034 SMPTE 292M / 259M adaptive cable equalizer is a monolithic integrated circuit for equalizing data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 143 Mbps to 1.485 Gbps and supports SMPTE 292M, SMPTE 344M and SMPTE 259M.

The CLC034 implements DC restoration to correctly handle pathological data conditions. DC restoration can be bypassed for low data rate applications. The equalizer is flexible in allowing either single-ended or differential input drive.

Additional features include a combined carrier detect and output mute pin which mutes the output when no signal is present. A programmable mute reference is used to mute the output at a selectable level of signal degradation. A cable length indicator is provided to determine the amount of cable being equalized.

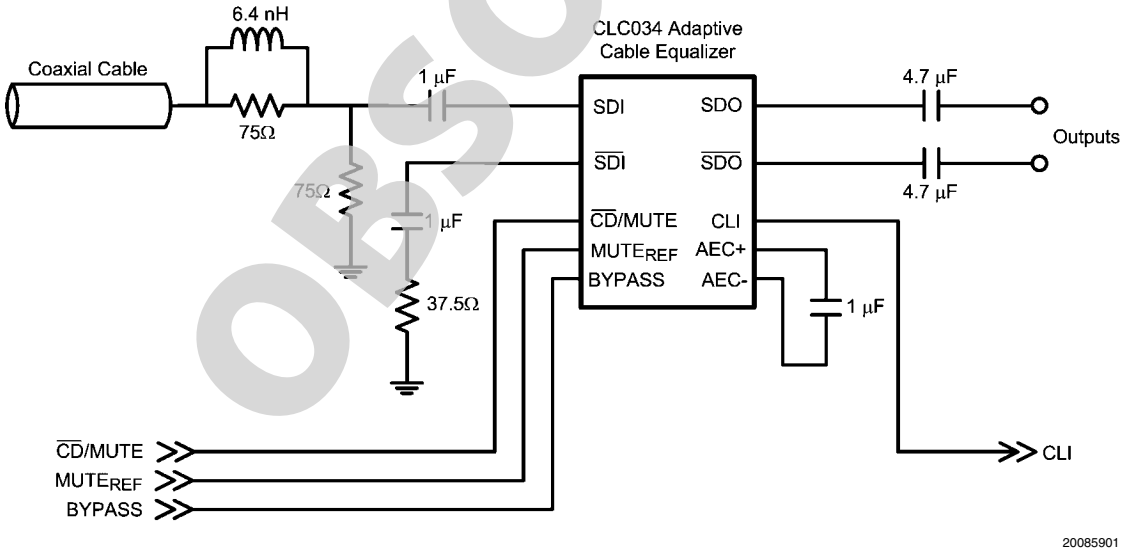
Features

- SMPTE 292M, SMPTE 344M and SMPTE 259M compliant
- Supports DVB-ASI at 270 Mbps
- High data rates: 143 Mbps to 1.485 Gbps
- Equalizes up to 140 meters of Belden 1694A at 1.485 Gbps or up to 350 meters of Belden 1694A at 270 Mbps
- Manual bypass, cable length indicator, and output mute with a programmable threshold
- Single-ended or differential input
- 50Ω differential outputs
- Single 3.3V supply operation
- 208mW typical power consumption with 3.3V supply
- Replaces the GS1524 and GS1524A

Applications

- SMPTE 292M, SMPTE 344M, and SMPTE 259M serial digital interfaces
- Serial digital data equalization and reception
- Data recovery equalization

Typical Application



Absolute Maximum Ratings (*Note 1*)

Supply Voltage	−0.5V to 3.6V
Input Voltage (all inputs)	−0.3V to V_{CC}+0.3V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering 4 Sec)	+260°C
Package Thermal Resistance	
θ_{JA} 16-pin SOIC	+115°C/W
θ_{JC} 16-pin SOIC	+105°C/W
ESD Rating (HBM)	8kV
ESD Rating (MM)	250V

Recommended Operating Conditions

Supply Voltage (V_{CC} – V_{EE})	3.3V ±5%
Input Coupling Capacitance	1.0 µF
AEC Capacitor (Connected between AEC+ and AEC-)	1.0 µF
Operating Free Air Temperature (T_A)	0°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (*Note 2*, *Note 3*).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{CMIN}	Input Common Mode Voltage		SDI, $\overline{SDI}$		1.9		V
V_{SDI}	Input Voltage Swing	At CLC034 input, 1.485 Gbps, T_A= +25°C to +85°C, $\overline{CD}$/MUTE may be used, (*Note 4*, *Note 6*)		720	800	880	mV_{P-P}
		At CLC034 input, 270 Mbps, T_A= +25°C to +85°C, $\overline{CD}$/MUTE may be used, (*Note 4*, *Note 6*, *Note 7*)		720	800	830	mV_{P-P}
		At CLC034 input, 143 to 1485 Mbps, $\overline{CD}$/MUTE tied to GND (MUTE disabled), (*Note 4*, *Note 6*, *Note 7*)		720	800	950	mV_{P-P}
V_{CMOUT}	Output Common Mode Voltage		SDO, $\overline{SDO}$		V_{CC} – V_{SDO}/2		V
V_{SDO}	Output Voltage Swing	50Ω load, differential			750		mV_{P-P}
	CLI DC Voltage	0m cable	CLI		2.5		V
		no signal			1.2		V
	$MUTE_{REF}$ DC Voltage (floating)		$MUTE_{REF}$		1.3		V
	$MUTE_{REF}$ Range				0.7		V
	$\overline{CD}$/MUTE Output Voltage	Carrier not present	$\overline{CD}$/MUTE	2.6			V
		Carrier present				0.4	V
	$\overline{CD}$/MUTE Input Voltage	Min to mute outputs		3.0			V
		Max to force outputs active				2.0	V
I_{CC}	Supply Current	(*Note 8*)			63	77	mA

200859 Version 5 Revision 2 Print Date/Time: 2011/09/21 14:51:16

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (*Note 3*).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
BR_{SDI}	Input Data Rate		SDI, $\overline{SDI}$	143		1485	Mbps
	Maximum Equalized Cable Length (with equalizer pathological)	270 Mbps, Belden 1694A, 0.2UI output jitter, (*Note 4*)			350		m
		270 Mbps, Belden 8281, 0.2UI output jitter, (*Note 4*)			280		m
		1.485 Gbps, Belden 1694A, 0.25UI output jitter, (*Note 4*)			140		m
		1.485 Gbps, Belden 8281, 0.25UI output jitter, (*Note 4*)			100		m
t_r,t_f	Output Rise Time, Fall Time	20% – 80%, (*Note 4*)	SDO, $\overline{SDO}$		100	220	ps
	Mismatch in Rise/Fall Time	(*Note 4*)			2	15	ps
t_{OS}	Output Overshoot	(*Note 4*)			1	5	%
R_{OUT}	Output Resistance	single-ended, (*Note 5*)			50		Ω
RL_{IN}	Input Return Loss	(*Note 9*)	SDI, $\overline{SDI}$	15	18-20		dB
R_{IN}	Input Resistance	single-ended			1.3		kΩ
C_{IN}	Input Capacitance	single-ended, (*Note 5*)			1		pF

Note 1: "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Note 2: Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.

Note 3: Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.

Note 4: Specification is guaranteed by characterization.

Note 5: Specification is guaranteed by design.

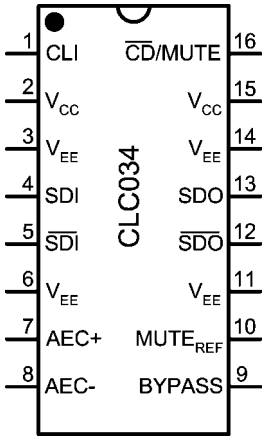
Note 6: The maximum input voltage swing assumes a nonstressing, DC-balance signal; specifically, the SMPTE-recommended color bar test signal. Pathological or other stressing signals may not be used. This specification is for 0m cable only.

Note 7: The CLC034 is fully compatible with the 800mV_{P-P} ±10% SMPTE 259M generator specification when $\overline{CD}$/MUTE is tied to GND (MUTE is disabled). For 143 Mpbs input, $\overline{CD}$/MUTE should always be tied to GND.

Note 8: Supply current depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased. Refer to Figures 1, 2.

Note 9: Input return loss is dependent on board design. The CLC034 meets this specification on the SD034 evaluation board from 5MHz to 1.5GHz.

Connection Diagram

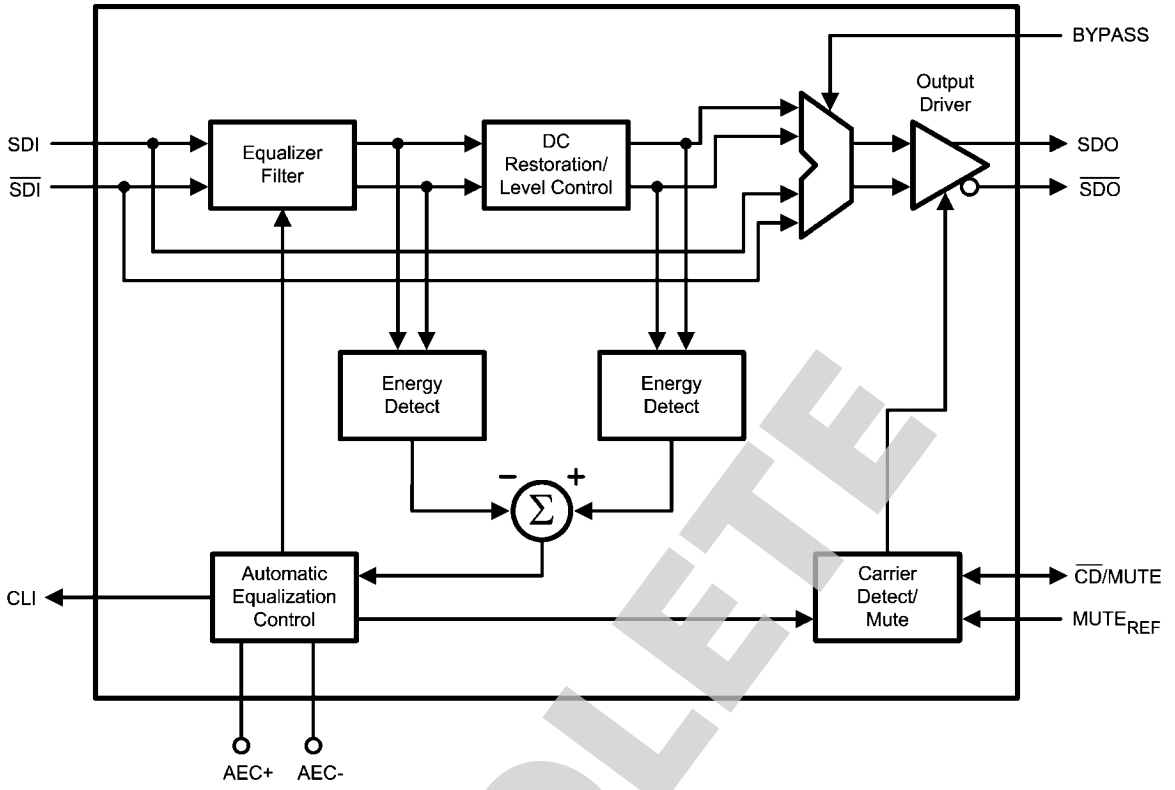


16-Pin SOIC
Order Number CLC034MA
See NS Package Number M16A

Pin Descriptions

Pin #	Name	Description
1	CLI	Cable length indicator. Provides a voltage inversely proportional to the cable length being equalized.
2	V_{CC}	Positive power supply (+3.3V).
3	V_{EE}	Negative power supply (ground).
4	SDI	Serial data true input.
5	$\overline{SDI}$	Serial data complement input.
6	V_{EE}	Negative power supply (ground).
7	AEC+	AEC loop filter external capacitor (1µF) positive connection.
8	AEC-	AEC loop filter external capacitor (1µF) negative connection.
9	BYPASS	Bypasses equalization and DC restoration when high. No equalization occurs in this mode.
10	$MUTE_{REF}$	Mute reference. Determines the maximum cable to be equalized before muting. May be unconnected for maximum equalization.
11	V_{EE}	Negative power supply (ground).
12	$\overline{SDO}$	Serial data complement output.
13	SDO	Serial data true output.
14	V_{EE}	Negative power supply (ground).
15	V_{CC}	Positive power supply (+3.3V).
16	$\overline{CD}$/MUTE	Bi-directional carrier detect and output mute. $\overline{CD}$/MUTE is high when no signal is present. If unconnected, MUTE is controlled automatically by carrier detect. To force MUTE on, tie to V_{CC}. To disable MUTE, tie to GND. $\overline{CD}$/MUTE has no function in BYPASS mode.

Block Diagram



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Device Operation

BLOCK DESCRIPTION

The **Equalizer Filter** block is a multi-stage adaptive filter. If Bypass is high, the equalizer filter is disabled.

The **DC Restoration / Level Control** block receives the differential signals from the equalizer filter block. This block incorporates a self-biasing DC restoration circuit to fully DC restore the signals. If Bypass is high, this function is disabled.

The signals before and after the DC Restoration / Level Control block are used to generate the **Automatic Equalization Control (AEC)** signal. This control signal sets the gain and bandwidth of the equalizer filter. The loop response in the AEC block is controlled by an external 1µF capacitor placed across the AEC+ and AEC- pins. **Cable Length Indicator (CLI)** is derived from this block.

The **Carrier Detect / Mute** block generates the carrier detect signal and controls the mute function of the output. This block utilizes the bi-directional **$\overline{\text{CD}}$/MUTE** signal along with **Mute Reference (MUTE_{REF})**.

The **Output Driver** produces SDO and $\overline{\text{SDO}}$.

CABLE LENGTH INDICATOR (CLI)

The cable length indicator provides a voltage to indicate the length of cable being equalized. The CLI voltage decreases as the cable length increases.

MUTE REFERENCE (MUTE_{REF})

The mute reference determines the amount of cable to equalize before automatically muting the outputs. This is set by applying a voltage inversely proportional to the length of cable to equalize. As the applied MUTE_{REF} voltage is increased, the amount of cable that can be equalized before carrier detect is de-asserted and the outputs are muted is decreased. MUTE_{REF} may be left unconnected for maximum equalization before muting.

CARRIER DETECT / MUTE ($\overline{\text{CD}}$/MUTE)

Carrier Detect / Mute is bi-directional, serving as both a carrier detect (output function) and mute (input function).

When used as an output, $\overline{\text{CD}}$/MUTE determines if a valid signal is present at the CLC034 input. If MUTE_{REF} is used, the carrier detect threshold will be altered accordingly. $\overline{\text{CD}}$/MUTE provides a high voltage when no signal is present at the CLC034 input, and the outputs are automatically muted. This is true if no cable is connected to the input or if the input cable is very long, typically 450m Belden 1694A for 1.485 Gbps input or 550m Belden 1694A for 270 Mbps input (with standard 800 $\text{mV}_{\text{P-P}}$ color bar input signals). $\overline{\text{CD}}$/MUTE is low when a valid input signal has been detected, and the outputs are automatically enabled.

As an input, $\overline{\text{CD}}$/MUTE can be used to override the carrier detect and manually mute or enable the CLC034 outputs. Applying a high input to $\overline{\text{CD}}$/MUTE will mute the CLC034 outputs. Applying a low input will force the outputs to be active regardless of the length of cable or the state of MUTE_{REF}.

INPUT INTERFACING

The CLC034 accepts either differential or single-ended input. The input must be AC coupled. Transformer coupling is not supported.

The CLC034 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in SMPTE RP 178 and RP 198, respectively.

OUTPUT INTERFACING

The SDO and $\overline{SDO}$ outputs are internally loaded with 50Ω. They produce a 750 mV_{P-P} differential output, or a 375 mV_{P-P} single-ended output.

Application Information

PCB LAYOUT RECOMMENDATIONS

Please refer to the following Application Note on National's website: **AN-1372, "CLC034 PCB Layout Techniques."**

REPLACING THE GENNUM GS1524

The CLC034 is footprint compatible with the Gennum GS1524 and GS1524A.

SUPPLY CURRENT VS. CABLE LENGTH

The supply current (I_{CC}) depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased. *Figure 1* shows supply current vs. Belden 1694A cable length for 1.485 Gbps data and *Figure 2* shows supply current vs. Belden 1694A cable length for 270 Mbps data.

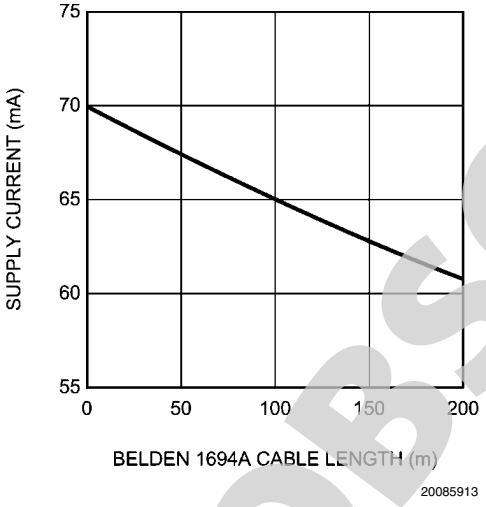


FIGURE 1. Supply Current vs. Belden 1694A Cable Length, 1.485 Gbps

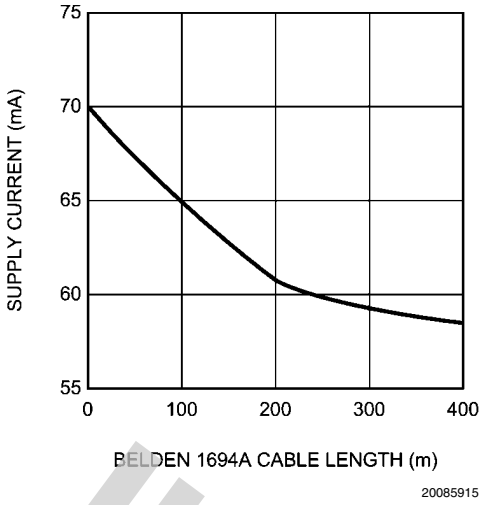


FIGURE 2. Supply Current vs. Belden 1694A Cable Length, 270 Mbps

ADDITIONAL DETAILS FOR USING CARRIER DETECT / MUTE FEATURE

Table 1 outlines the equalizer input operating conditions based on zero meters of cable length. This is not a condition normally seen in standard applications of SDI equalizers. Typically there is some length of cable between the signal source and the equalizer (hence the need for equalization). Any cable length will attenuate (reduce) the SDI signal amplitude from the amplitude transmitted at the source. The table specifies voltage levels measured at the input of the equalizer which is equivalent to a zero meter cable length from the signal source.

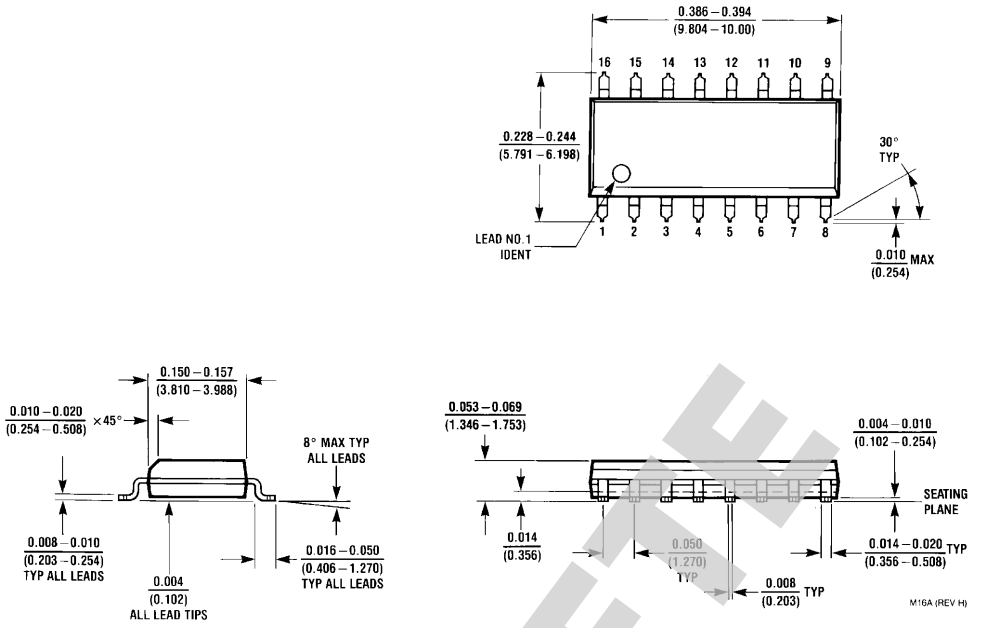
The output will mute if the SDI input signal (V_{SDI}) exceeds the maximum input voltage (V_{SDI} max). Disable $\overline{CD}$/MUTE (tie it to GND) to avoid unwanted muting of the output.

TABLE 1. V_{SDI} Conditions for Proper $\overline{CD}$/MUTE Use vs. Input Data Rate

Input Data Rate (Mbps)	Conditions if $\overline{CD}$/MUTE Used	Conditions if $\overline{CD}$/MUTE Disabled($\overline{CD}$/MUTE Tied to GND)
143, 177	Do not use $\overline{CD}$/MUTE (tie it to GND)	Acceptable V_{SDI}: 720 to 950 mV_{P-P}(all input data rates)
270, 360, 540	Acceptable V_{SDI}: 720 to 830 mV_{P-P} (*Note 10*)	
1485	Acceptable V_{SDI}: 720 to 880 mV_{P-P}	

Note 10: For 270 Mbps input data rates, the CLC034's maximum acceptable V_{SDI} is only 0.5 dB below the SMPTE 259M specified 880 mV_{P-P} amplitude for zero meters cable. A 10m length of Belden 8281 cable attenuates the signal enough for SMPTE 259M compliance.

Physical Dimensions inches (millimeters) unless otherwise noted



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Notes

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LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
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