- **Support for 6-Bit as Well as 8-Bit Video Inputs, With On-Chip Dithering**
- **FlatLink™ Input Interface for Low EMI and Power**
- **mini-LVDS Intra-Panel Interface Towards Column Drivers**
- **DE-Only Mode of Operation**
- **Tolerates Spread Spectrum Clock at the Input, With SSC Pass-Thru to the Outputs**
- **Support for SSC at the Outputs by Using External SSC Generation**
- **Flexible Control Outputs With User-Programmable Timings**
- **Support for 2-Level and 3-Level Gate Drivers**
- **Optional Serial EEPROM for Fine Tuning Timing During Development**
- **Four Default Timing Sets Provided On-Chip**
- **Fail-Safe Circuit Detects Off-Spec Conditions and Generates Timing Signals Internally**
- **PowerPAD™ TQFP Package**
- **Operating Voltage Range: 2.7 V to 3.6 V**

description

The TFP74X3 is a family of programmable timing controllers for TFT LCD panels supporting resolutions from XGA up to QXGA. The timing controllers reside on the panel and provide the interface between graphics controllers and the TFT-LCD system, routing video data and generating timing signals for the panel.

The host interface is FlatLink, which is a proven, low-power, and low-EMI serial interface. mini-LVDS, an advanced serial intra-panel interface, is used between the TFP74X3 and the column drivers, resulting in improved EMI performance and lower power consumption.

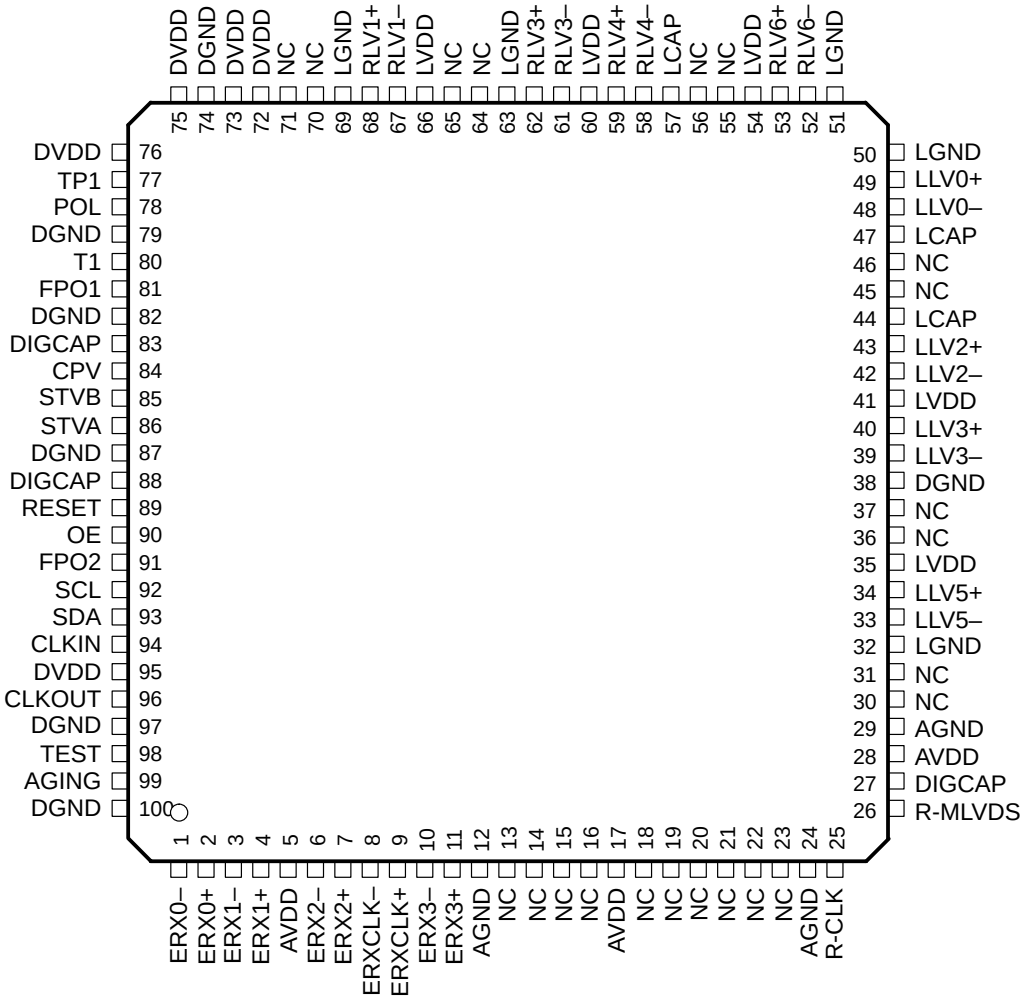
Control outputs with user-programmable timings are available to control source and gate drivers. Additional control outputs are available to sequence the panel power supplies. The TFP74X3 can be configured from an optional external serial EEPROM.

PACKAGE INFORMATION

DEVICE	RESOLUTIONS SUPPORTED	PACKAGE
TFP7423	XGA	100-pin TQFP
TFP7433	SXGA, SXGA+	100-pin TQFP
TFP7443	UXGA	100-pin TQFP
TFP7453	QXGA	100-pin TQFP

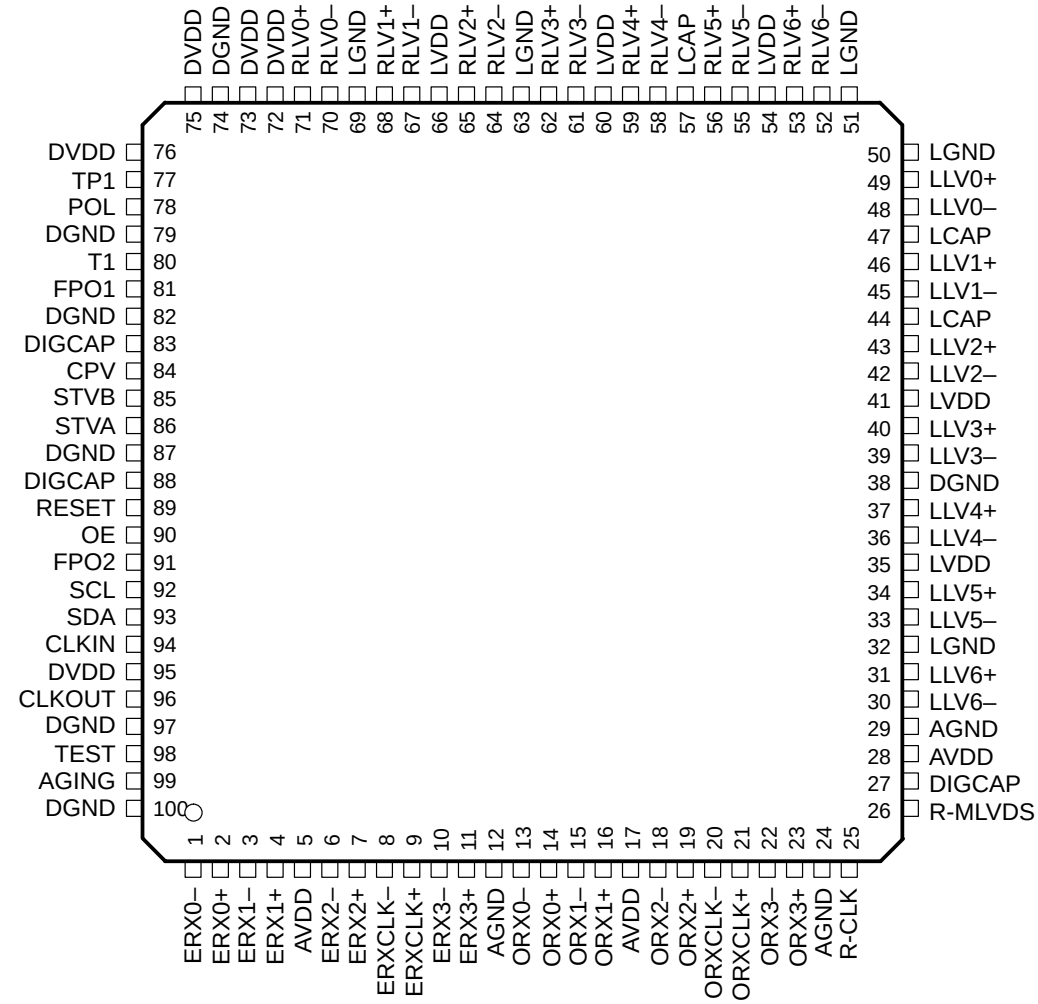
pin assignment for TFP7423

TQFP PACKAGE
(TOP VIEW)

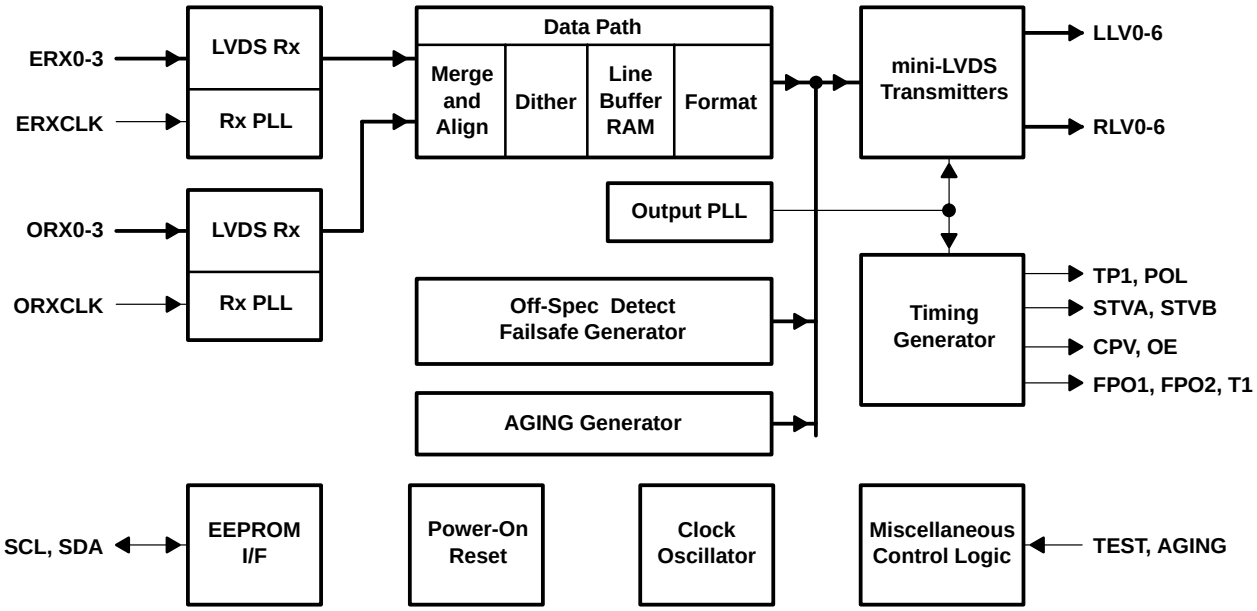


pin assignment for TFP7433, TPF7443, and TFP7453

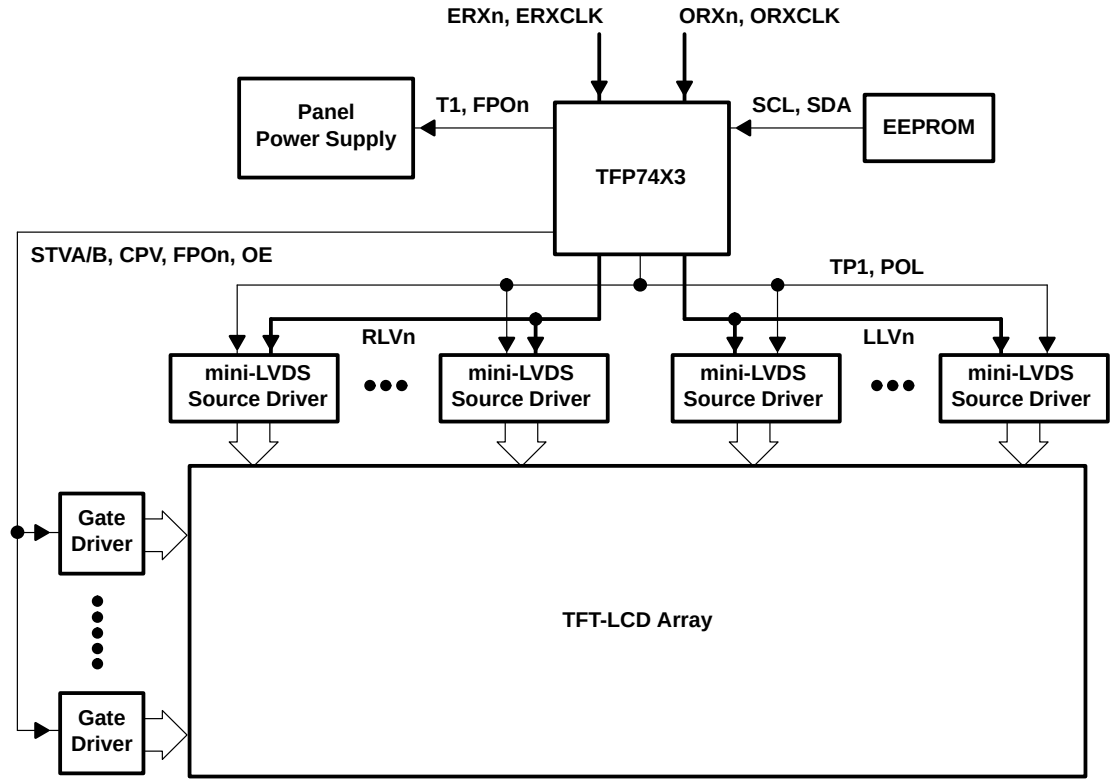
TQFP PACKAGE
(TOP VIEW)



block diagram



system diagram



Terminal Functions

FlatLink inputs†

TERMINAL			TYPE	DESCRIPTION
NAME	NO.			
	TFP7423	TFP74x3		
ERX0±...ERX3±	1, 2, 3, 4, 6, 7, 10, 11	1, 2, 3, 4, 6, 7, 10, 11	Differential inputs	Even pixel FlatLink (LVDS) data inputs. This is the port used in single-port mode. In dual-port mode, the first pixel is input to this port.
ERXCLK±	8, 9	8, 9	Differential input	Clock pair for even-pixel port
ORX0±...ORX3±		13-16, 18, 19, 22, 23	Differential inputs	Odd pixel FlatLink (LVDS) data inputs. This port is unused in single-port mode.
ORXCLK±		21, 20	Differential input	Clock pair for odd-pixel port
NC	13-16, 18-23			Not connected

† All the FlatLink signals have to be terminated with external resistors. See Figure 1 for the data format on the FlatLink ports.

mini-LVDS outputs

TERMINAL			TYPE	DESCRIPTION
NAME	NO.			
	TFP7423	TFP74x3		
LLV0±…LLV6±	49, 48, 43, 42, 40, 39, 34, 33	49, 48, 46, 45, 43, 42, 40, 39, 37, 36, 34, 33, 31, 30	Differential outputs	mini-LVDS outputs. mini-LVDS clock pairs are assigned out of these pins depending on the mode/resolution. Drive levels for data pins are set by a resistor on R-MLVDS. Drive levels for clock pins are set proportional to the data pin drive levels by a register. Pre-emphasis levels are programmable by registers.
RLV0±…RLV6±	68, 67, 62, 61, 59, 58, 53, 52	71, 70, 68, 67, 65, 64, 62, 61, 59, 58, 56, 55, 53, 52		
NC	30, 31, 36, 37, 45, 46, 55, 56, 64, 65. 70, 71			Not connected

source driver control signals

TERMINAL			TYPE	DESCRIPTION
NAME	NO.			
	TFP7423	TFP74x3		
POL	78	78	Output CMOS 4 mA	Polarity control. Output with reference to TIP1. Programmable for dot-inversion or 2-line inversion by register.
TP1	77	77		Rising edge generated after all the line data is fed out on mini-LVDS pairs. Width programmable by register.

EEPROM interface

TERMINAL			TYPE	DESCRIPTION
NAME	NO.			
	TFP7423	TFP74x3		
SCL, SDA	92, 93	92, 93	Open-drain I/O	I^2C interface pins for connecting to external EEPROM. If an EEPROM is not present, then these pins are used as inputs to select from one of four built-in timing sets.

Terminal Functions (Continued)

power pins

TERMINAL			TYPE	DESCRIPTION
NAME	NO.			
	TFP7423	TFP74x3		
AGND	12, 24, 29	12, 24, 29		Analog ground
AVDD	5, 17, 28	5, 17, 28		Power supply for the analog circuitry (PLLs).
DGND	38, 74, 79, 82, 87, 97, 100	38, 74, 79, 82, 87, 97, 100		Digital ground
DIGCAP	27, 83, 88	27, 83, 88		External capacitor for on-chip 1.8-V regulator for the digital logic. Each DIGCAP pin requires their own capacitor to DGND.
DVDD	72, 73, 75, 76, 95	72, 73, 75, 76, 95		Power supply for the digital circuitry.
LCAP	44, 47, 57	44, 47, 57		External capacitor for on-chip 1.8-V regulator for the mini-LVDS transmitters. Each LCAP pin requires their own capacitor to LGND.
LGND	32, 50, 51, 63, 69	32, 50, 51, 63, 69		Ground connection for the mini-LVDS outputs.
LVDD	35, 41, 54, 60, 66	35, 41, 54, 60, 66		Power supply for the mini-LVDS outputs.

gate driver control signals

TERMINAL			TYPE	DESCRIPTION
NAME	NO.			
	TFP7423	TFP74x3		
CPV	84	84	Output CMOS 4 mA	Shift clock for gate driver. Rising and falling edges programmable around TP1 rising edge by registers. CPV starting time (after power-on) is programmable by register.
FPO1	81	81	Output CMOS 4 mA	Fully programmable general-purpose output. Can be used for OE2, frame pulse, or dc-dc control. Programmable using registers.
FPO2	91	91		
OE	90	90	Output CMOS 4 mA	Output enable for gate driver. Rising and falling edges programmable around TP1 rising edge by registers. Polarity of OE after power on is programmable.
STVA	86	86	Output CMOS 4 mA	Gate strobe. Pulse width, duration, and position with respect to the first line is programmable using registers.
STVB	85	85		

Figure 2 is an example of typical waveforms that can be generated on the gate driver control outputs. For details on programming the timings of these signals, see the *EEPROM register assignment and definition* section.

Terminal Functions (Continued)

miscellaneous

TERMINAL			TYPE	DESCRIPTION
NAME	NO.			
	TFP7423	TFP74x3		
AGING	99	99	Input	In AGING mode, built-in video patterns are fed out on the mini-LVDS outputs. L = Auto-graying patterns are output H = Normal operation Internally pulled up AGING mode requires external clock to be fed in at the FlatLink ports. Note: The status of AGING is sensed only at power on.
CLKIN	94	94	Input	Dot-clock fed in after spreading. If external SSC is not being done, then CLKOUT can be connected to CLKIN internally by register programming. In that case, CLKOUT buffer is powered down.
CLKOUT	96	96	Output CMOS 8 mA	Recovered dot-clock brought out, to feed to external SSC chip.
R-CLK	25	25	Analog output	External resistor to GND sets internal clock oscillator frequency. The frequency can be set between 6 MHz and 12 MHz.
R-MLVDS	26	26	Analog output	External resistor to GND sets drive level (steady state) on mini-LVDS data pairs. The drive level can be set up to 8 mA.
RESET	89	89	Schmitt trigger input	Used for power-on reset with external resistor and capacitor.
TEST	98	98	Input	Controls whether the TFP74X3 is in normal operation mode. H = test mode, L = normal operation.
T1	80	80	Output CMOS 4 mA	Can be used to control panel dc-dc converter. Starting time after power on is programmable with register.

detailed description

LVDS receiver

The FlatLink receiver has two input ports. ERX0– through ERX3– and ERX0+ through ERX3+ are for the even (0, 2, 4…) pixels, ORX0– through ORX3– and ORX0+ through ORX3+ are for the odd (1, 3, 5…) pixels. In the single input port mode, ERX0– through ERX3– and ERX0+ through ERX3+ must be used. Both 18-bit color and 24-bit color are supported.

The FlatLink inputs are SSC tolerant and input SSC is passed on to the outputs to enable a low-EMI total solution.

NOTE:

The TFP7423 has only one input port.

data path

In the data path, video data from the two input ports are aligned and merged to form a single data stream. On-chip dithering is available to convert 24-bit color to 18-bit color. The dithering can be turned on or off by the user through the use of suitable register programming. The formatting section adds control bits to the mini-LVDS data stream and distributes data to different mini-LVDS outputs depending on resolution and mounting options. For normally-black panels, the video data can be inverted by register programming.

mini-LVDS transmitter

There are 14 pairs of mini-LVDS outputs, arranged as seven pairs for the left half-bus (LLV0– through LLV6– and LLV0+ through LLV6+) and seven pairs for the right half-bus (RLV0– through RLV6– and RLV0+ through RLV6+). Data and clock pairs are assigned out of these pins depending on the mode/resolution. Drive levels for data pairs are set by a resistor on R-MLVDS. The drive levels on the clock pairs can be set proportional to the data-pair drive levels by register programming. Pre-emphasis with register-programmable levels may be used on the mini-LVDS signals.

timing generator

The timing generator produces signals for controlling the gate drivers, source drivers, and the panel power supply. The timing signals can be programmed by configuring the internal registers from an external EEPROM. Two versatile general-purpose outputs, FPO1 and FPO2, are also available.

fail-safe circuit and clock oscillator

The TFP74X3 detects if the input signal is out of specification. In such a case, the fail-safe circuit generates timing signals and feeds black data to the panel. This prevents any damage to the panel. The fail-safe circuit works off an internal clock. The frequency of the internal oscillator is set by a single external resistor.

EEPROM interface

This block controls the reading of an external I^2C EEPROM. If an EEPROM is not connected, the TFP74X3 configures itself from one of four internal ROMs, depending on how the SCL and SDA pins are connected (pulled high/pulled low). In case an external EEPROM is connected, but the read operation is not successful, the TFP74X3 remains in the reset condition.

miscellaneous control logic

This block configures the internal registers from the EEPROM (if present) and sets up the internal control depending on the contents of the EEPROM, the status of SCL, SDA, TEST, and AGING.

power-on reset

A laser-trimmed band-gap voltage sets accurate thresholds for the power-on reset. An external resistor and capacitor set the reset duration. Internal circuitry in this block also detects glitches in the power supply and initiates a reset sequence if a glitch in the power supply reduces voltage below safe levels, preventing damage to the panel.

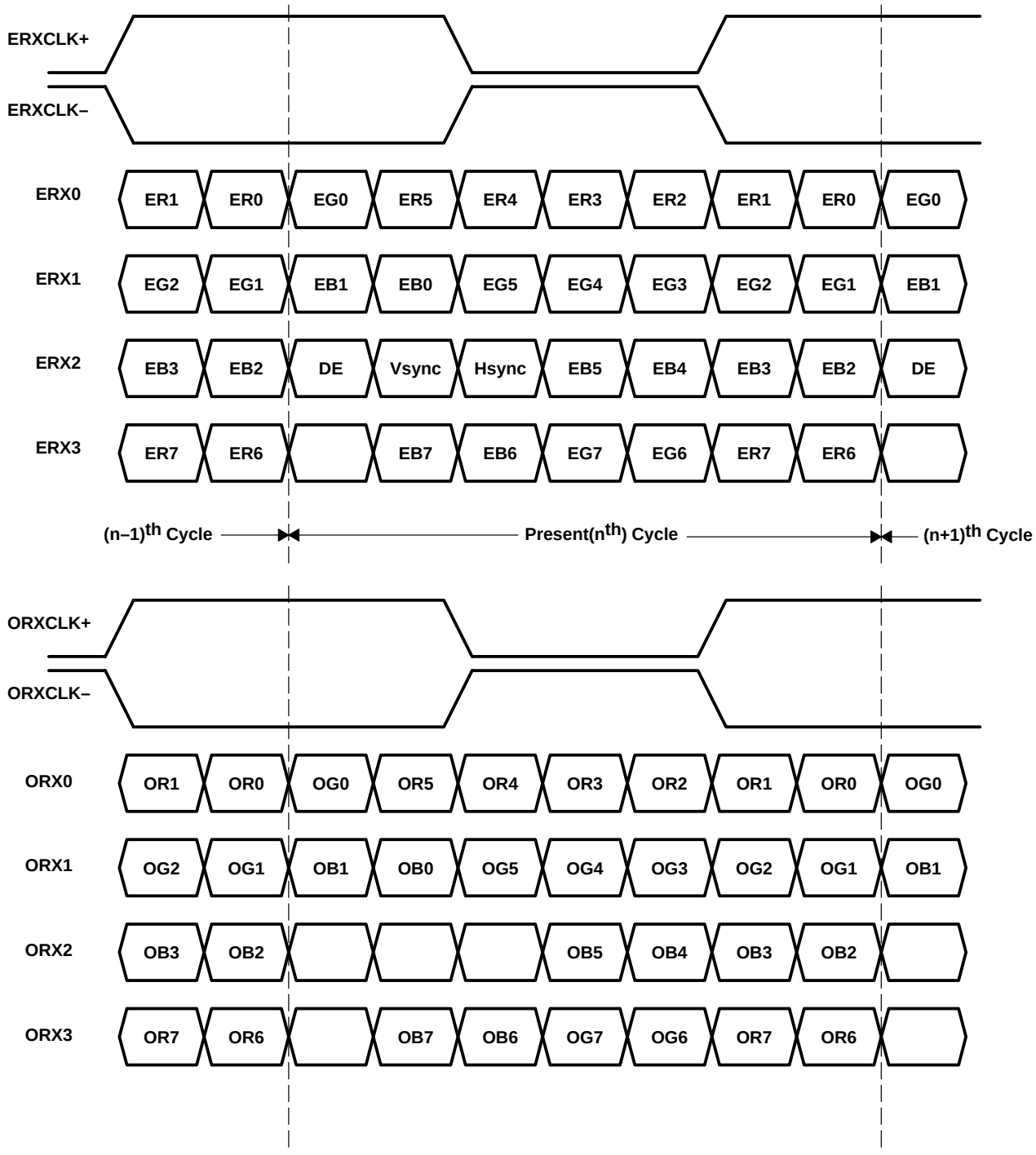


Figure 1. FlatLink Data Mapping

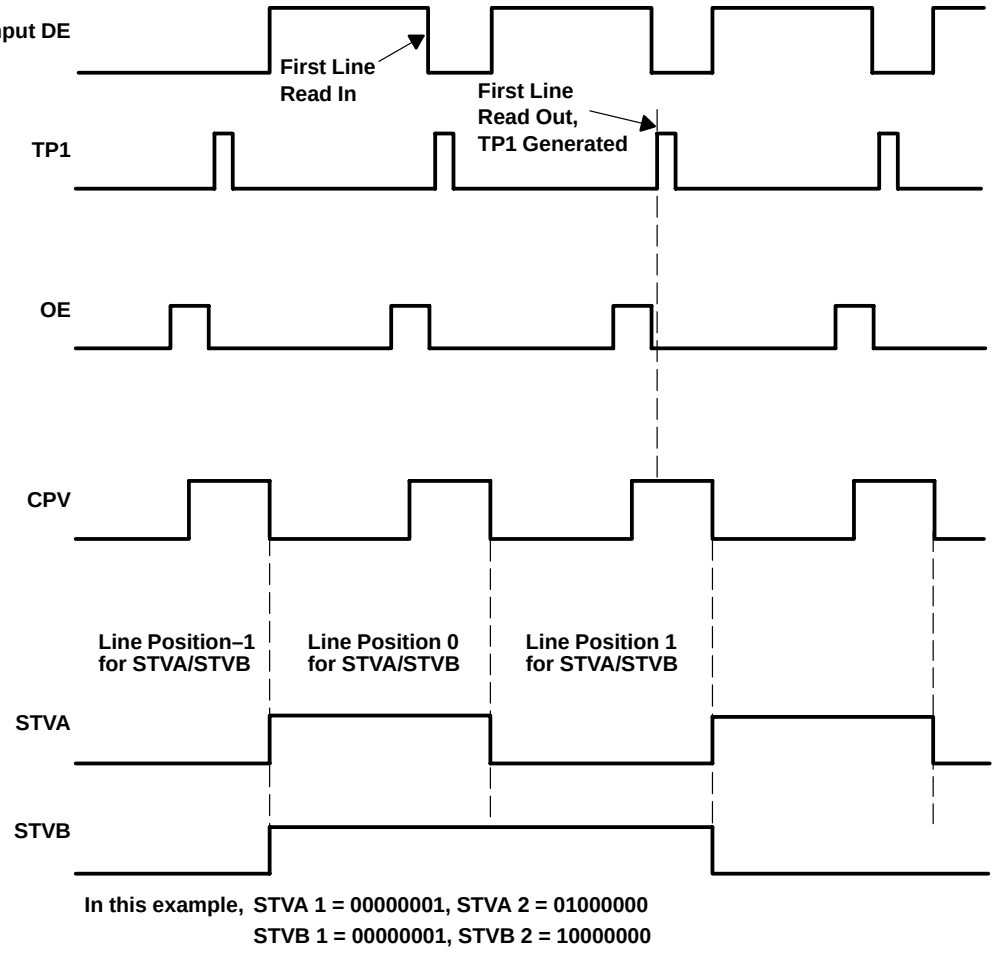


Figure 2. Timing of Normal Operation

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage DVDD, AVDD, LVDD		–0.5 V to 4 V
Input voltage:	FlatLink pins	–0.5 V to 2.6 V
	mini-LVDS outputs	–0.1 V to 2.6 V
	DIGCAP	1.8 V to 2.6 V
	All other pins	–0.5 V to VDD + 0.5 V
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature 1,5 mm from case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals unless otherwise noted.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}	DVDD, AVDD, LVDD	2.7	3.3	3.6	V
High-level input voltage, V_{IH}	Digital inputs, SDA	$0.7V_{DD}$			V
Low-level input voltage, V_{IL}	Digital inputs, SDA			$0.3V_{DD}$	V
Differential input voltage, $\|V_{ID}\|$	FlatLink inputs	50		600	mV
Common-mode input voltage, V_{IC}	FlatLink inputs	$\frac{0.6 + \|V_{ID}\|}{2}$	1.2	$\frac{2 - \|V_{ID}\|}{2}$	V
mini-LVDS drive level (steady state), I_{SS}	LLV0–7, RLV0–7			8	mA
Internal clock frequency, f_{OSC}		6	10	12	MHz
Input clock frequency, $f_{(clk)}$	ERXCLK, ORXCLK	40		112	MHz
Modulating frequency of input clock during SSC, f_{MOD}	ERXCLK, ORXCLK			200	kHz
Maximum deviation of input clock frequency during SSC, f_{DEV}	ERXCLK, ORXCLK			±2%	
Reset duration, $t_{(RST)}$			10		ms
TP1 width, T_HTP		1			$t_{(R)}$
Pullup resistors, R_P	SCL, SDA		4.7		kΩ
Ambient temperature, T_A		0		70	°C

NOTE: For values of $t_{(R)}$ and $t_{(M)}$, see the *mini-LVDS outputs* and the *gate and source driver control outputs* sections.

electrical characteristics over recommended operating conditions (unless otherwise specified)

TP1, POL, CPV, OE, FPO1, FPO2, STVA, STVB, T1, SCL

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 4 mA	2.3			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V

CLKOUT

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 8 mA	2.3			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V

CLKIN, TEST

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN}	Input current	V_{IN} = 0 V to V_{DD}			10	μA

AGING

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Input current	V_{IL} = 0 V			800	μA

RESET (see Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN}	Input current	V_{IN} = 0 V to V_{DD}			1	μA
$V_{(TH)}$	Reset threshold voltage		2.3	2.4	2.5	V
V_{hys}	Hysteresis voltage			50		mV

electrical characteristics over recommended operating conditions (unless otherwise specified) (continued)

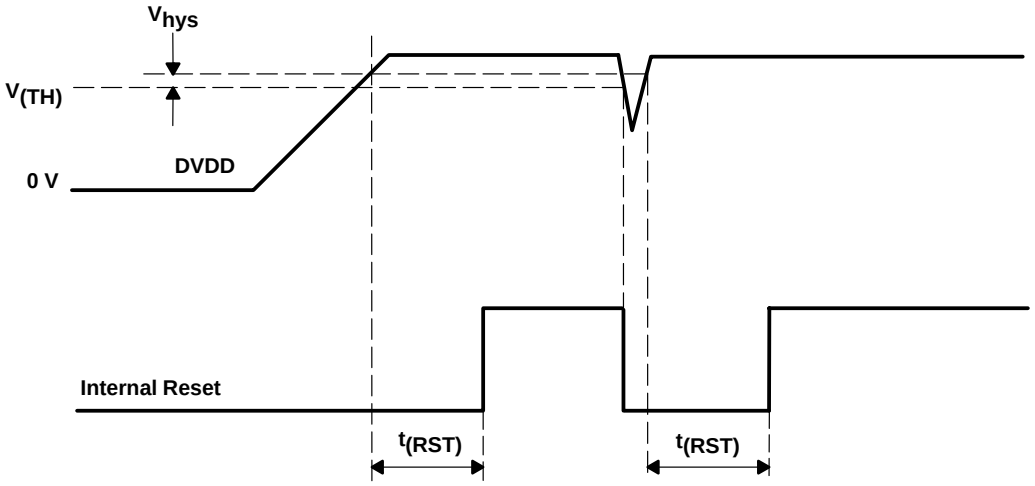


Figure 3. Power-On Reset and Glitch Detect

FlatLink ports

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{IC} = 1.2 V			50	mV
V_{IT-}	Negative-going input threshold voltage	V_{IC} = 1.2 V	–50			mV
I_{IN}	Input current				10	μA

mini-LVDS outputs (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OCM}	Common-mode output voltage		1.1	1.2	1.3	V
I_{SS}	Drive level (steady state)				8	mA
$I_{(PK)}$	Peak drive level		1		1.6	I_{SS}
$R_{(TERM)}$	mini-LVDS termination resistance		50		150	Ω

NOTE: $I_{(PK)} \times R_{(TERM)}$ should not exceed 800 mV

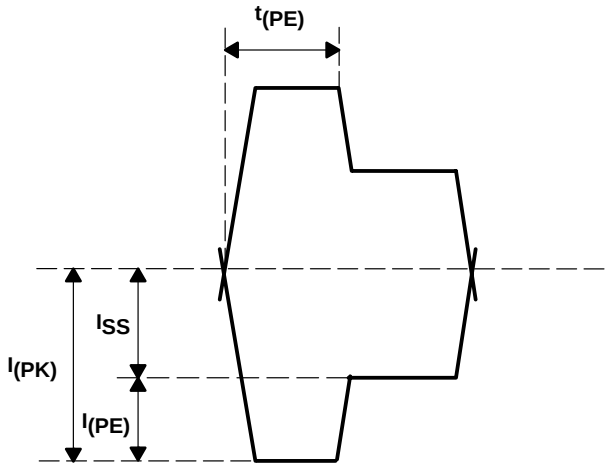


Figure 4. mini-LVDS Outputs

ac electrical characteristics over recommended operating conditions (unless otherwise specified)

FlatLink inputs (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(SW)}$	Sampling window				650	ps
$t_{sk(RSKM)}$	Receiver skew margin	$f_{(CLK)}$ = 82 MHz	540			ps
$t_{sk(EO)}$	Skew - even to odd port		–3/7		3/7	t_C

mini-LVDS outputs (see Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(MH)}$	Clock high time			$t_{(M)}/2$		
$t_{(ML)}$	Clock low time			$t_{(M)}/2$		
t_{su}	Data setup time			$t_{(M)}/4$		
t_h	Data hold time			$t_{(M)}/4$		
$t_{(PE)}$	pre-emphasis duration			$t_{(M)}/4$		
t_t	Transition time				500	ps

source driver control outputs (TP1, POL) (see Figure 7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(TP)}$	Last mini-LVDS data to TP1 delay			11.5		$t_{(M)}$
$t_{(HTP)}$	TP1 high time		1		63	$t_{(R)}$
$t_{su(POL)}$	POL setup time to TP1			1		$t_{(M)}$

gate driver control outputs (CPV, STVA, STVB, OE) (see Figure 9)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(CPV)}$	TP1 to CPV rising		–127		127	$t_{(R)}$
$t_{f(CPV)}$	TP1 to CPV falling		–127		127	$t_{(R)}$
$t_{r(OE)}$	TP1 to OE rising		–127		127	$t_{(R)}$
$t_{f(OE)}$	TP1 to OE falling		–127		127	$t_{(R)}$
$t_{d(STV)}$	CPV to STVA/B delay			0		

T1, CPV, OE at power-on (see Figure 10)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(RST)}$	Reset duration			0.55RC		
$t_{(READ)}$	EEPROM read duration	f_{osc} = 10 MHz		5.2		ms
$t_{d(T1)}$	T1 activation delay time	f_{osc} = 10 MHz	0		155	ms
$t_{d(CPV)}$	CPV activation delay time	f_{osc} = 10 MHz	0		155	ms

EEPROM interface (see Figure 11)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency	f_{osc} = 7.5 MHz, R_P = 4.7 kΩ, C_L = 50 pF		46.5		kHz
$t_{(SCL\_H)}$	Clock high time		4.0			µs
$t_{(SCL\_L)}$	Clock low time		4.7			µs
$t_{r(EE)}$	SCL, SDA rise time				1000	ns
$t_{f(EE)}$	SCL, SDA fall time				300	ns
$t_{su(STA)}$	Start condition setup time		4.7			µs
$t_{h(STA)}$	Start condition hold time		4.0			µs
$t_{su(STP)}$	Stop condition setup time		4.0			µs
$t_{su(DAT)}$	Data setup time		250			ns
$t_{h(DAT)}$	Data hold time		300			ns
$t_{(BUF)}$	Bus free time		4.7			µs

EEPROM interface (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency	f_{osc} = 10 MHz, R_P = 4.7 kΩ, C_L = 50 pF		62		kHz
$t_{(SCL\_H)}$	Clock high time		4.0			µs
$t_{(SCL\_L)}$	Clock low time		4.7			µs
$t_{r(EE)}$	SCL, SDA rise time				1000	ns
$t_{f(EE)}$	SCL, SDA fall time				300	ns
$t_{su(STA)}$	Start condition setup time		3.5			µs
$t_{h(STA)}$	Start condition hold time		3.7			µs
$t_{su(STP)}$	Stop condition setup time		4.0			µs
$t_{su(DAT)}$	Data setup time		250			ns
$t_{h(DAT)}$	Data hold time		300			ns
$t_{(BUF)}$	Bus free time		4.7			µs

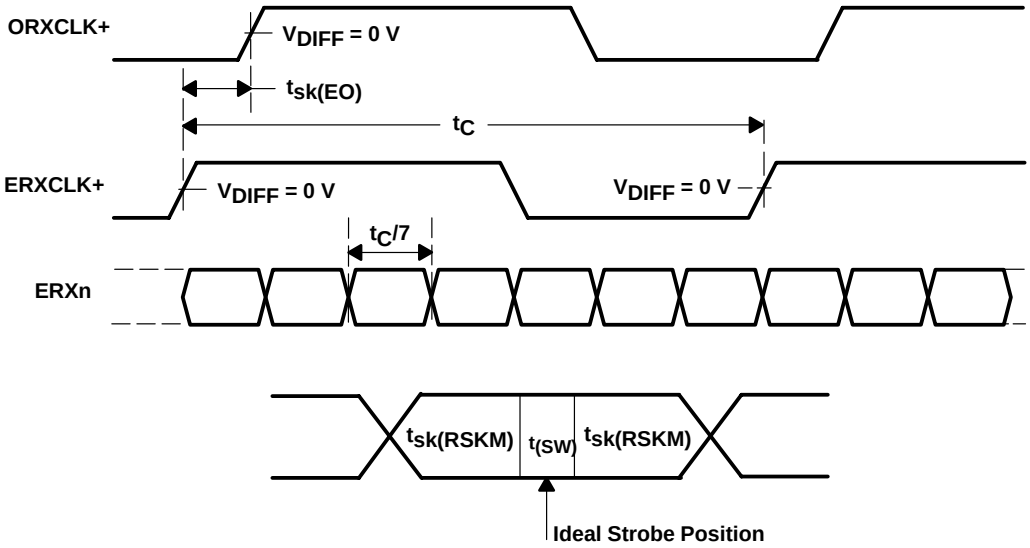


Figure 5. Input Timing

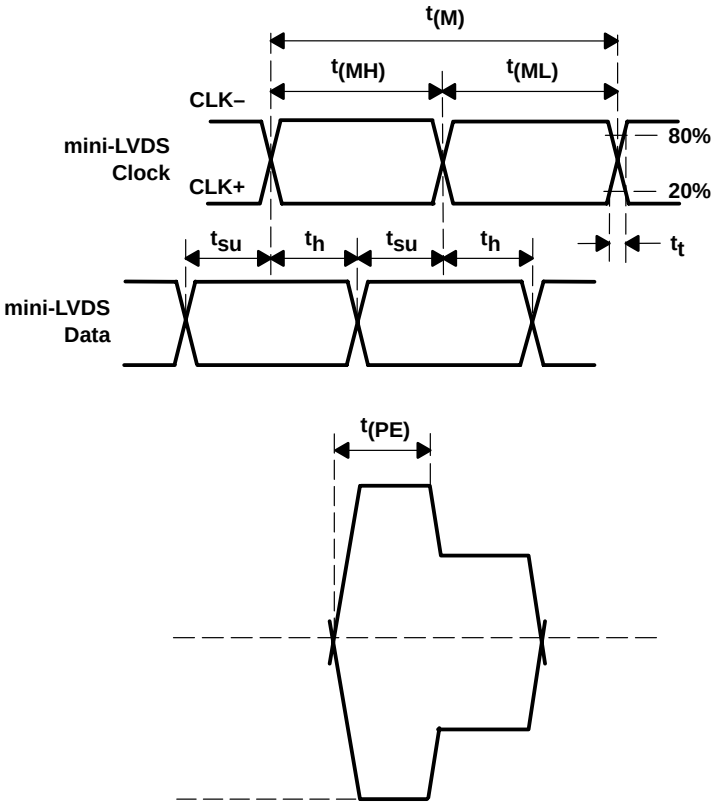


Figure 6. mini-LVDS Output Timing

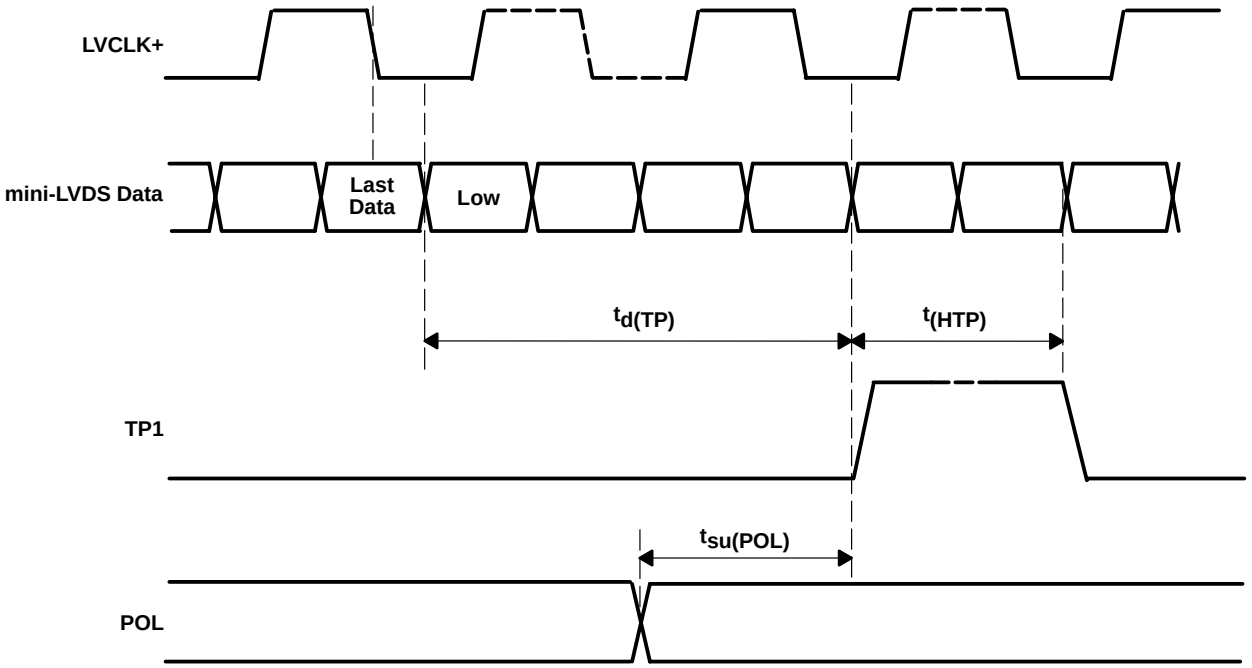


Figure 7. TP1, POL Timings

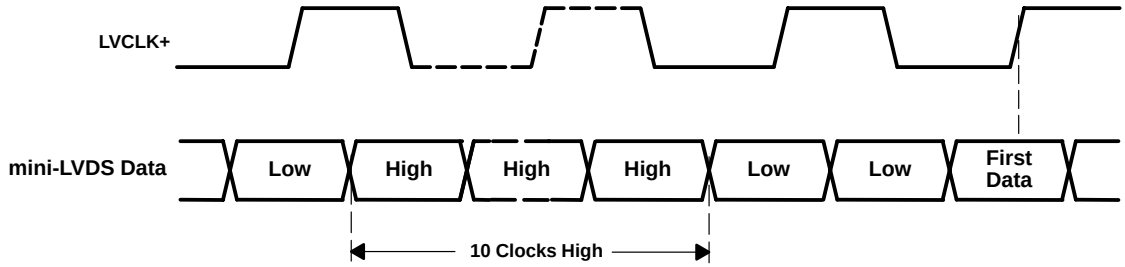


Figure 8. Reset Pulse Generation on mini-LVDS Data Pair

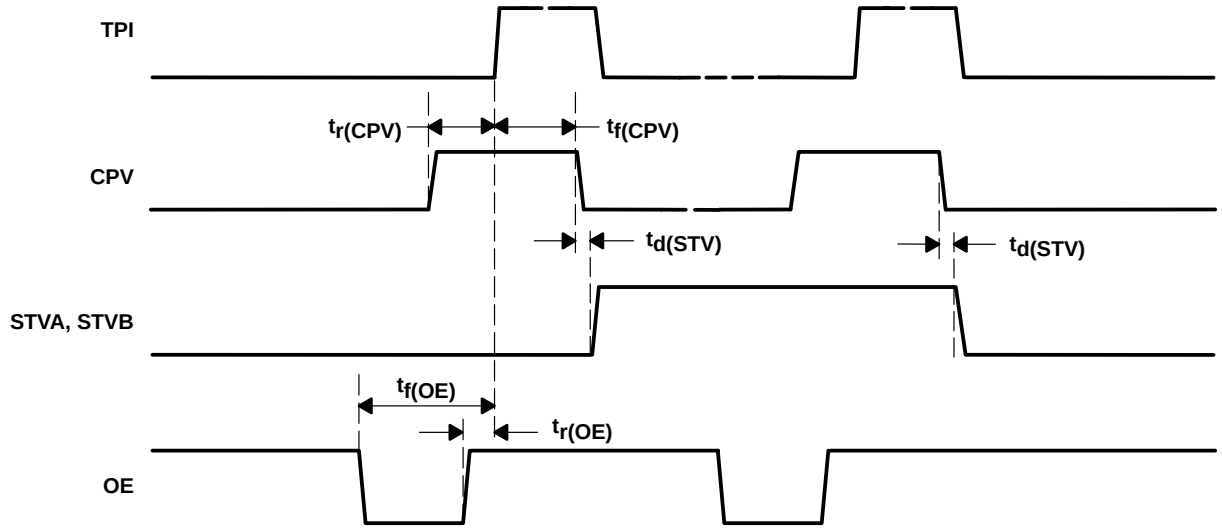


Figure 9. Gate Driver Control Timings

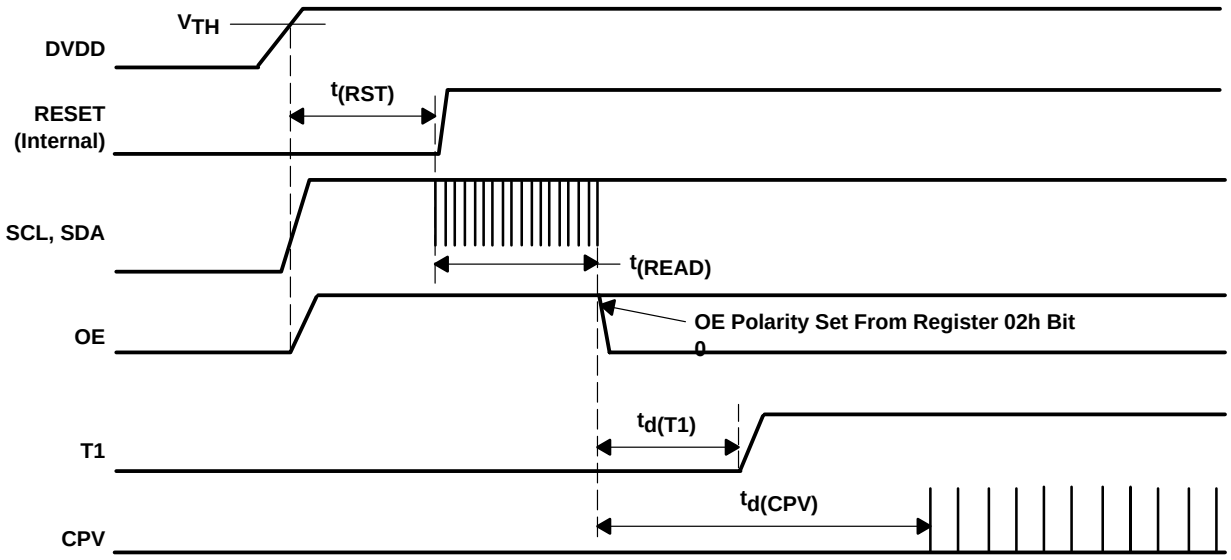


Figure 10. Signal Timings at Power On

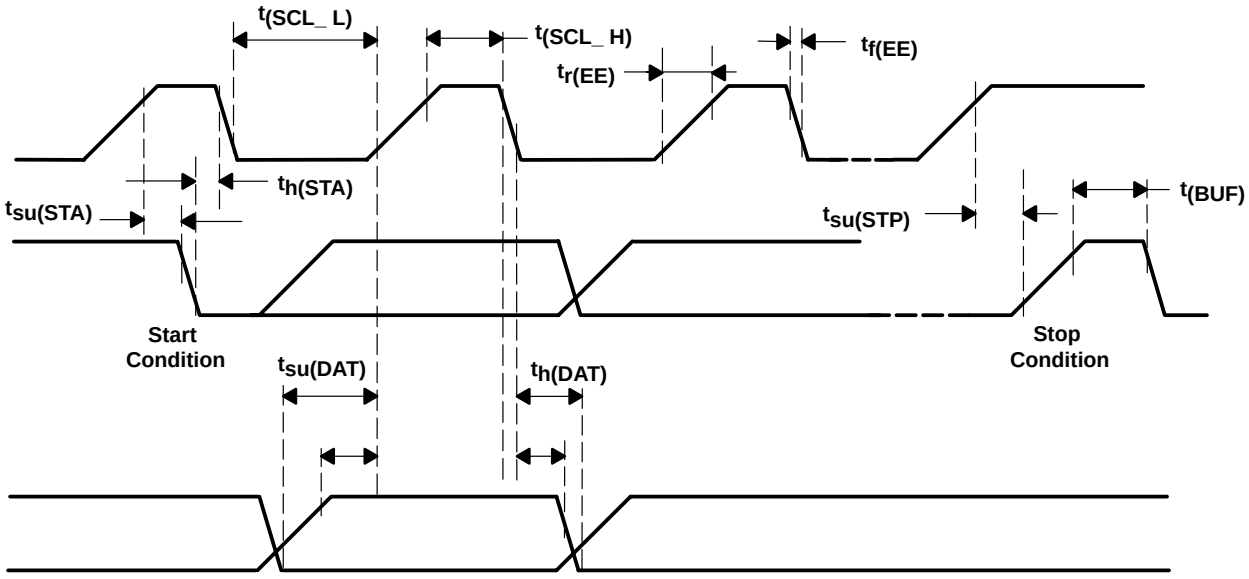


Figure 11. EEPROM Interface Timings

off-spec conditions

During normal display operation, the fail-safe circuitry in the TFP74X3 constantly checks for a valid input signal as well as input clock. If either the clock fails or if the signal becomes abnormal, the TFP74X3 enters auto-refresh mode and generates control signals for the source and gate drivers, at the same time feeding all black data on the mini-LVDS data pairs.

Any input signal not complying with the conditions listed in Table 1 and Table 2 forces the TFP74X3 into the auto-refresh mode.

Table 1. Specifications of Valid Input Signal in DE-Only Mode

	TOTAL NUMBER OF CLOCKS/LINE		TOTAL NUMBER OF LINES/FRAME		TOTAL NUMBER OF LINES/VBLANK	
	MIN	MAX	MIN	MAX	MIN	MAX
XGA	1088	2048	512	1536	4	
SXGA	1344	2048	512	1536	4	
SXGA+	1464	4096	1024	2046	4	
UXGA	1664	4096	1024	2046	4	
UXGA-FPT	1664	4096	1024	2046	4	
QXGA	2128	4096	1024	2046	6	

Table 2. Specifications of Valid Input Signal in H-Sync, V-Sync Mode

	TOTAL CLOCKS/LINE		TOTAL Hs/FRAME		TOTAL Hs/VB-bp		TOTAL Hs in VB	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
XGA	1088	2048	512	1536	4	126		
SXGA	1344	2048	512	1536	4	126		
SXGA+	1464	4096	1024	2046	4	126		
UXGA	1664	4096	1024	2046	5	126		
UXGA-FPT	1664	4096	1024	2046			4	126
QXGA	2128	4096	1024	2046			6	126

EEPROM register assignment and definition

Table 3. EEPROM Register Assignment and Definition

ADDRESS (Hex)	NAME	FUNCTION
00	Auto detect	If 10101010, EEPROM present. Else default mode
01	Format control 1	Sets resolutions, modes, etc.
02	Format control 2	Sets 6/8-bit mode, dithering, OE polarity, etc.
03	Drive levels	Sets pre-emphasis and mini-LVDS clock drive levels
04	T1 timing	Defines timing on T1 pin
05	CPV start	CPV start timer value
06	TP1 width	Programs TP1 width
07	CPV rising edge	Sets CPV timing with respect to TP1
08	CPV falling edge	Sets CPV timing with respect to TP1
09	OE timing 1	Sets OE timing with respect to TP1
0A	OE timing 2	Sets OE timing with respect to TP1
0B	STVA control 1	Sets STVA width and position in terms of line count
0C	STVA control 2	Sets STVA width and position in terms of line count
0D	STVB control 1	Sets STVB width and position in terms of line count
0E	STVB control 2	Sets STVB width and position in terms of line count
0F	Off-spec checks	Enables/disables various off-spec checks
10	FPO1 control	Sets FPO1 mode
11	FPO1 start	Sets FPO1 first transition
12	FPO1 stop	Sets FPO1 second transition
13	FPO2 control	Sets FPO2 mode
14	FPO2 start	Sets FPO2 first transition
15	FPO2 stop	Sets FPO2 second transition
16	Auto-refresh TP1	Sets TP1 width during auto-refresh
17	Auto-refresh CPV low	Sets duration of CPV low during auto-refresh
18	Auto-refresh CPV high	Sets duration of CPV high during auto-refresh
19	Auto-refresh OE timing 1	Sets OE timing with respect to CPV in auto-refresh
1A	Auto-refresh OE timing 2	Sets OE timing with respect to CPV in auto-refresh
1B	Reserved	
1C	Reserved	
1D	Reserved	
1E	Reserved	
1F	Check-sum	Check-sum of EEPROM contents from 00h to 1Eh

Table 4. Format Control 1

[2–0]	000 = XGA 001 = SXGA 010 = SXGA+ 011 = UXGA 100 = UXGA FPT 110 = QXGA			
[3]	0 = single input port, 1 = dual input ports			
[4]	Should be 0			
[5]	Video signal inversion. 0 = signal not inverted, 1 = signal inverted			
[6]	2-line POL control. 0 = Dot inversion, 1 = 2-line inversion			
[7]	TCON position. 0 = top mount, 1 = bottom mount (see Figure 23)			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	10101110	10001010	10001011	10000000

Table 5. Format Control 2

[0]	OE polarity after EEPROM read			
[2–1]	Gate driver initialization at power on 00 = 0 frame initialization 01 = 1 frame initialization 10 = 2 frames initialization 11 = 3 frames initialization			
[3]	Determines the method of the timing signal generation in Vblank 0 = H-sync is used to generate signals (should be used if the input has a spread spectrum) 1 = Signals are generated internally, using the stored value of the line length			
[4]	0 = 6-bit input, 1 = 8-bit input			
[5]	0 = 6-bit output, 1 = 8-bit output			
[6]	0 = Disable dithering, 1 = enable dithering If dithering is disabled and input is 8 bits and output is 6 bits, then truncate.			
[7]	0 = Short CLKIN to CLKOUT, 1 = CLKIN and CLKOUT not connected			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00000001	00000001	00000001	00000011

Table 6. Drive Levels

[2–0]	Sets clock drive levels in terms of data drive levels. From 1x to 4x in steps of 0.5x 000....Clock drive level = 1 times data drive level 001....Clock drive level = 1.5 times data drive level ..... 110....Clock drive level = 4 times data drive level 111....Reserved
[3]	Determines the minimum operating frequency of the input PLL. 0 = Minimum frequency is 4 x f_{OSC} 1 = Minimum frequency is 2.8 x f_{OSC} (Recommended value = 1)
[5–4]	Sets data pre-emphasis drive levels in terms of data steady-state level. 00....No pre-emphasis 01....20% pre-emphasis 10....40% pre-emphasis 11....60% pre-emphasis

Table 6. Drive Levels (Continued)

[7–6]	Sets clock pre-emphasis drive levels in terms of clock steady-state level. 00....No pre-emphasis 01....20% pre-emphasis 10....40% pre-emphasis 11....60% pre-emphasis			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00000000	00000000	00000000	00000000

Table 7. T1 Timing

[4–0]	Sets timing of transition from 0 ms to 155 ms in 5-ms increments			
[7–5]	Reserved			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00000001	00000001	00000001	00001010

Table 8. CPV Start

[4–0]	Sets start timing of CPV pulses from 0 ms to 155 ms in 5-ms increments			
[7–5]	Reserved			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00000010	00000011	00000011	00001111

Table 9. TP1 Width

[5–0]	Controls TP1 width from 1 $t_{(R)}$ to 63 $t_{(R)}$			
[7–6]	Reserved			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00000101	00001000	00001100	00010011

Table 10. CPV Rising Edge

[6–0]	Sets CPV rising edge with reference to TP1 rising edge from 0 $t_{(R)}$ to 127 $t_{(R)}$.			
[7]	0 = transition after TP1 edge, 1 = transition before TP1 edge			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	10100101	00000000	10111000	00010011

Table 11. CPV Falling Edge

[6–0]	Sets CPV falling edge with reference to TP1 rising edge from 0 $t_{(R)}$ to 127 $t_{(R)}$			
[7]	0 = transition after TP1 edge, 1 = transition before TP1 edge			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00101111	00101000	00111101	10111001

Table 12. OE Timing 1

If OE power-on polarity is high (bit 0 of register 02h = 1), then this register defines the OE falling edge timing. If OE power-on polarity is low (bit 0 of register 02h = 0), then this register defines the OE rising edge timing.				
[6–0]	Sets OE edge with reference to TP1 rising edge from 0 $t_{(R)}$ to 127 $t_{(R)}$			
[7]	0 = transition after TP1 edge, 1 = transition before TP1 edge			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00000101	00001000	00000000	00010111

Table 13. OE Timing 2

If OE power-on polarity is high (bit 0 of register 02h = 1), then this register defines the OE rising edge timing. If OE power-on polarity is low (bit 0 of register 02h = 0), then this register defines the OE falling edge timing.				
[6–0]	Sets OE edge with reference to TP1 rising edge from 0 $t_{(R)}$ to 127 $t_{(R)}$			
[7]	0 = transition after TP1 edge, 1 = transition before TP1 edge			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	10110100	10101000	10111101	00000110

NOTE: If OE timing 1 and OE timing 2 are programmed to the same value, the OE remains at the value set by register bit 02[0].

Table 14. STVA Control 1 and Control 2

Together, STVA control 1 and STVA control 2 determine the generation of the STVA pulses. The range is from –7 to 8. A 1 in the bit position enables the generation of a pulse in the corresponding line.				
STVA 1 [7–0]	Bit 7 = line number –7, Bit 0 = line number 0			
STVA 2 [7–0]	Bit 7 = line number 1, Bit 0 = line number 8			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
1	00000111	00000111	00000111	00000001
2	00000000	00000000	00000000	00000000

Table 15. STVB Control 1 and Control 2

Together, STVB control 1 and STVB control 2 determine the generation of the STVB pulses. The range is from –7 to 8. A 1 in the bit position enables the generation of a pulse in the corresponding line.				
STVB 1 [7–0]	Bit 7 = line number –7, Bit 0 = line number 0			
STVB 2 [7–0]	Bit 7 = line number 1, Bit 0 = line number 8			
Built-in Default Value	**ROM0**	**ROM1**	**ROM2**	**ROM3**
1	00000001	00000011	00000011	00000000
2	00000000	10000000	10000000	10000000

Table 16. Off-Spec Check

[0]	Dot clock	0 = ignore loss of dot-clock, 1 = check			
[1]	Clocks / line	0 = ignore H-sync frequency, 1 = check			
[2]	H-sync / frame	0 = ignore V-sync frequency, 1 = check			
[3]	H-sync / VB back porch	0 = ignore # H-sync in VB back-porch, 1 = check			
[4]	H-sync / Vblank	0 = ignore # H-sync in Vblank , 1 = check			
[5]	Clocks / line (DE only)	0 = ignore clocks / line, 1 = check			
[6]	Lines / frame (DE only)	0 = ignore lines / frame, 1 = check			
[7]	Lines / Vblank (DE only)	0 = ignore lines / Vblank, 1 = check			
Built-in Default Values		**ROM0**	**ROM1**	**ROM2**	**ROM3**
		00010111	00001111	00000111	11100001

Table 17. FPO1 Control

[7]	Pulse polarity			
[6–5]	00 = Pulse is dc 01 = Pulse per frame 10 = Pulse per line			
[4–0]	Starting time of pulse activation after power on, from 0 ms to 155 ms in 5-ms steps.			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00000010	00000010	00000010	11000000

Table 18. FPO1 Start

[7–0]	Ignored in dc mode. In the once per frame mode, starting position of pulse = [7–0] = –127 to 127 with reference to the first line. ([7] = 1 indicates before first line) In the once per line mode, similar to OE start programming.			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00000000	00000000	00000000	00010111

Table 19. FPO1 Stop

[7–0]	Ignored in dc mode In the once per frame mode, stop position of pulse = [7–0] = –127 to 127 with reference to the last line. ([7] = 1 indicates before last line) In the once per line mode, similar to OE stop programming.			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00000000	00000000	00000000	10000011

Table 20. FPO2 Control

[7]	Pulse polarity			
[6–5]	00 = Pulse is dc 01 = Pulse per frame 10 = Pulse per line			
[4–0]	Starting time of pulse activation after power-on, from 0 ms to 155 ms in 5-ms steps.			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00000011	00000011	00000011	11000000

Table 21. FPO2 Start

[7–0]	Ignored in dc mode In the once per frame mode, starting position of pulse = [7–0] = –127 to 127 with reference to the first line. ([7] = 1 indicates before first line) In the once per line mode, similar to OE start programming.			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00000000	00000000	00000000	00010111

Table 22. FPO2 Stop

[7–0]	Ignored in dc mode In the once per frame mode, stop position of pulse = [7–0] = –127 to 127 with reference to the last line. ([7] = 1 indicates before last line) In the once per line mode, similar to OE stop programming.			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00000000	00000000	00000000	10000011

Table 23. Auto-Refresh TPI Width

[5–0]	Controls TP1 width during auto-refresh from 1 t_{osc} to 63 t_{osc}			
[7–6]	Reserved			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00010000	00010000	00010000	00011001

Table 24. Auto-Refresh CPV Low

[7–0]	Sets CPV low duration during auto refresh from 5 t_{osc} to 255 t_{osc}			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	01011111	01011111	01011111	10010011

Table 25. Auto-Refresh CPV High

[7–0]	Sets CPV high duration during auto-refresh from 2 t_{osc} to 255 t_{osc} Note: CPV high duration has to be greater than TP1 width			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00100111	00100111	00100111	00111100

Table 26. Auto-Refresh OE Timing 1

If OE power-on polarity is high (bit 0 of register 02h = 1), then this register defines the OE falling edge timing. If OE power-on polarity is low (bit 0 of register 02h = 0), then this register defines the OE rising edge timing.				
[6–0]	Sets OE edge with reference to CPV rising edge from 0 t_{osc} to 127 t_{osc}			
[7]	0 = transition after CPV rising edge, 1 = transition before CPV rising edge.			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	00010100	00010100	00010100	00011111

NOTE: If [7] = 0, then the value in [6–0] should be ≤ the value programmed for CPV auto-refresh high duration (register 18h).
If [7] = 1, then the value in [6–0] should be ≤ value programmed for CPV auto-refresh low duration (register 17h).

Table 27. Auto-Refresh OE Timing 2

If OE power-on polarity is high (bit 0 of register 02h = 1), then this register defines the OE rising edge timing. If OE power-on polarity is low (bit 0 of register 02h = 0), then this register defines the OE falling edge timing.				
[6–0]	Sets OE edge with reference to CPV rising edge from 0 t_{osc} to 127 t_{osc}			
[7]	0 = transition after CPV rising edge, 1 = transition before CPV rising edge.			
Built-in Default Values	**ROM0**	**ROM1**	**ROM2**	**ROM3**
	10001000	10001000	10001000	10001100

NOTE: If [7] = 0, then the value in [6–0] should be ≤ the value programmed for CPV auto-refresh high duration (register 18h).
If [7] = 1, then the value in [6–0] should be ≤ value programmed for CPV auto-refresh low duration (register 17h).
If auto-refresh OE timing 1 and auto-refresh timing 2 are programmed to the same value, the OE remains at the value set by register bit 02[0] during auto-refresh.

APPLICATION INFORMATION

register configuration from EEPROM/internal ROMs

The EEPROM should be configured at slave address 1010001.

On power up, the TFP74X3 examines the status of the SCL and SDA pins. If either of these are low, the TFP74X3 configures itself from the internal ROMs as shown below. If SCL and SDA are both high, the TFP74x3 attempts to configure itself from the external EEPROM. If there is no acknowledgement signal from the EEPROM, the values from ROM3 are used for configuring the registers.

If there is an acknowledgement signal, but the first byte read is not 10101010, the TFP74X3 pulls all outputs low and remains in a reset state. If the first byte is 10101010, the TFP74X3 loads its internal registers from the next 31 bytes of the EEPROM. If the check-sum verification is successful, the TFP74X3 starts operation; otherwise it turns all outputs off.

SCL	SDA	ROM #
0	0	ROM0
0	1	ROM1
1	0	ROM2
1	1	ROM3

In addition to the internal ROMs, an extra customizable area can be programmed at device manufacture time based on end-user requirements. Once timings have been optimized using the EEPROM, they can be *burnt in* into the device.

NOTE:
Once the device has been customized, the internal ROMs cannot be used.

Conceptually, the scheme looks like:

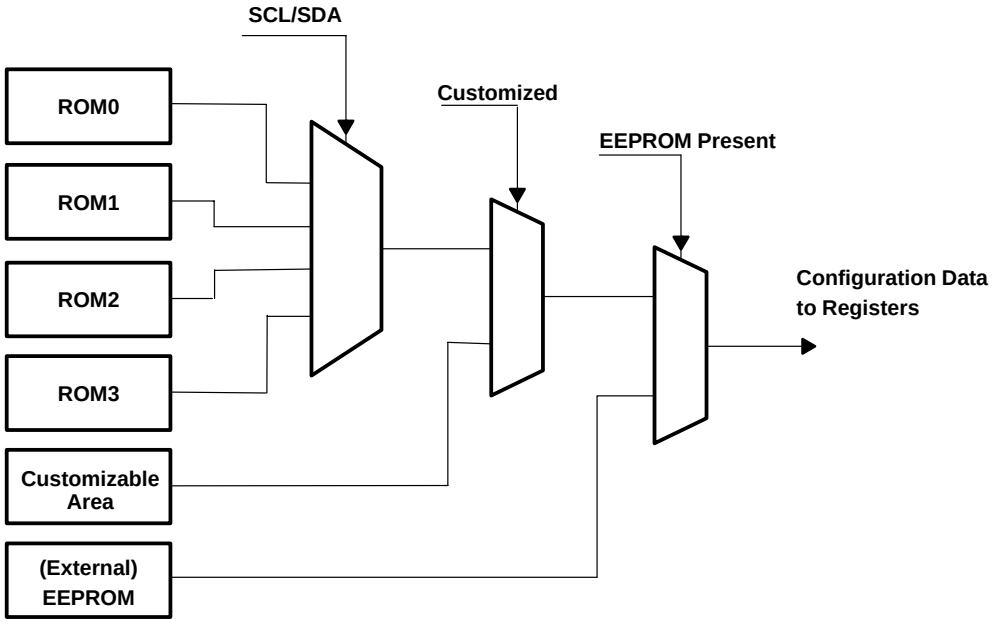


Figure 12. EEPROM Scheme

EEPROM address configuration

The EEPROM should be configured at slave address 1010001.

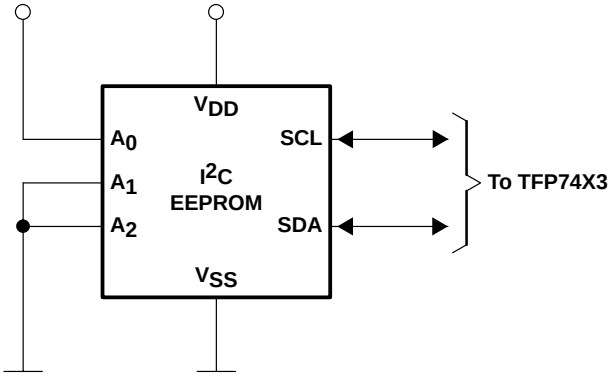


Figure 13. EEPROM Address Configuration

The EEPROM used for configuring the TFP74X3 cannot be shared for any other purpose (e.g. EDID).

APPLICATION INFORMATION

checksum algorithm

The algorithm used for generating the checksum is:

1. Add the contents of all locations from 00h to 1Eh (binary addition with carry).
2. Invert (complement) the result.
3. Add binary 1 to the result (with carry).
4. Use the lower 8 bits of this as checksum and program it into location 1Fh.

FlatLink inputs

Each of the FlatLink pairs has to be terminated in an external resistor, mounted as close as possible to the TFP74X3.

The port usage and nominal operating frequencies are specified inTable 28.

Table 28. Port Usage and Nominal Operating Frequencies

	SINGLE INPUT PORT	DUAL INPUT PORTS
XGA 60 Hz	65 MHz	NA
SXGA 60 Hz	108 MHz	54 MHz
SXGA+ 60 Hz	108 MHz	54 MHz
UXGA 60 Hz	NA	81 MHz
QXGA 50 Hz	NA	82 MHz

mini-LVDS outputs

Clock and data pairs are internally assigned out of the pool of mini-LVDS outputs based on the resolution and mode programmed. The assignment for all the modes are shown in *mini-LVDS pin assignments in different modes* section.

The nominal frequencies ($f_{(M)}$) on the mini-LVDS clock pairs are shown in Table 29.

Table 29. Nominal Frequencies of the mini-LVDS Clock Pairs

	BUS WIDTH	$f_{(M)} : f_{(CLK)}$	$f_{(M)}$	$t_{(M)}$
XGA 6 bit	Three pairs	3 : 2	97 MHz	10.26 ns
XGA 8 bit	Three pairs	2 : 1	130 MHz	7.69 ns
SXGA 6 bit	Five pairs	9:10	97 MHz	10.28 ns
SXGA 8 bit	Six pairs	1 : 1	108 MHz	9.26 ns
SXGA+ 6 bit	Four pairs	9 : 8	121 MHz	8.23 ns
SXGA+ 8 bit	Four pairs	3 : 2	162 MHz	6.17 ns
UXGA 6 bit	Five pairs	9 : 10	146 MHz	6.86 ns
UXGA 8 bit	Six pairs	1 : 1	162 MHz	6.17 ns
QXGA 6 bit (50 Hz)	Six pairs	3 : 4	124 MHz	8.13 ns
QXGA 8 bit (50 Hz)	Six pairs	1 : 1	165 MHz	6.10 ns

An external resistor connected from R-MLVDS to GND sets the steady-state drive strength on data pairs of the mini-LVDS outputs. The drive strength as a function of the resistance is shown in Figure 14. The drive strength on the clock pairs is set by register 03h. This register also sets the pre-emphasis on the data and clock pairs.

APPLICATION INFORMATION

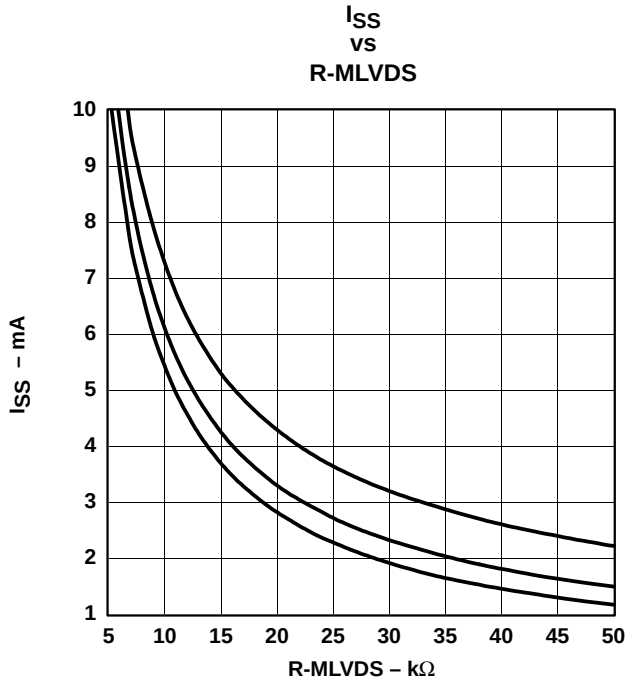


Figure 14. Drive Strength

gate and source driver control outputs

The timing resolution and range for various signals with programmable timings is described in Table 30 (absolute values are at nominal operating frequency).

Table 30. Timing Resolution and Range

MODE	RESOLUTION $t_{(R)}$	$t_{(R)}$ (nominal)	TP1 MAX WIDTH	CPV, OE EDGES
XGA 6	12 $t_{(M)}$	123.1 ns	7.75 µs	±15.6 µs
XGA 8	16 $t_{(M)}$	123.1 ns	7.75 µs	±15.6 µs
SXGA 6	8 $t_{(M)}$	82.2 ns	5.18 µs	±10.44 µs
SXGA 8	8 $t_{(M)}$	74.1 ns	4.67 µs	±9.41 µs
SXGA+ 6	9 $t_{(M)}$	74.1 ns	4.67 µs	±9.41 µs
SXGA+ 8	12 $t_{(M)}$	74.1 ns	4.67 µs	±9.41 µs
UXGA 6	8 $t_{(M)}$	54.9 ns	3.46 µs	±6.97 µs
UXGA 8	8 $t_{(M)}$	49.4 ns	3.11 µs	±6.27 µs
QXGA 6	6 $t_{(M)}$	48.8 ns	3.07 µs	±6.2 µs
QXGA 8	8 $t_{(M)}$	48.8 ns	3.07 µs	±6.2 µs

APPLICATION INFORMATION

internal oscillator frequency

A resistor connected from the R-CLK pin to GND sets the frequency of the internal oscillator. The frequency variation with resistance is shown in Figure 15.

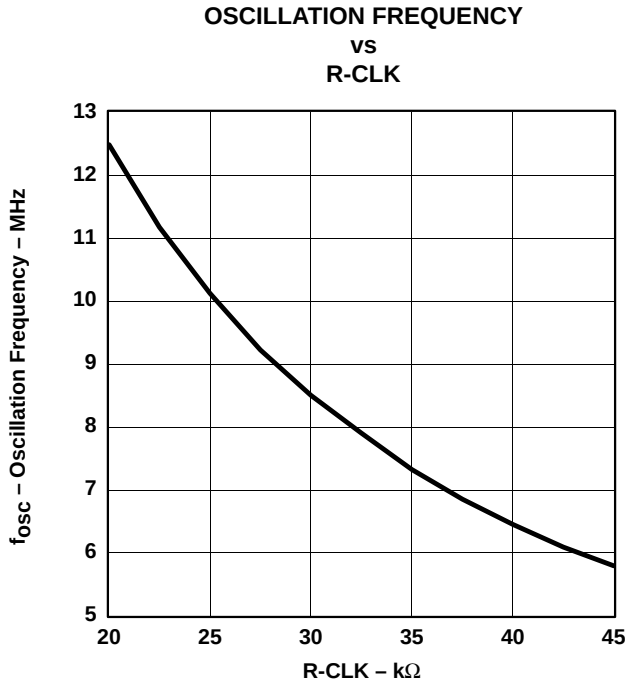


Figure 15. Frequency Variation With Resistance

FPO1 and FPO2

FPO1 and FPO2 are general-purpose outputs, which can be programmed by the user in a number of different ways:

- If programmed in dc mode, FPOn transitions once after power on. For example, if the polarity is programmed as H, then FPOn goes from low to high after a programmable delay after power-on reset. In this mode, FPOn can be used to sequence supply rails of the panel's dc/dc converter.
- When programmed in the once-per-line mode, the programming and behavior is identical to that of the OE pin.
- In the once-per-frame mode, FPOn generates a pulse every frame. The polarity of the pulse is programmable. The start position of the pulse is programmable around the first line, and the stop position is programmable with reference to the last line.

Figure 16 shows FPOn programmed with low polarity, start position at –2, and stop position at +1. The exact definition of position is similar to that of STVA/STVB and the transitions are aligned with the falling edge of CPV.

APPLICATION INFORMATION

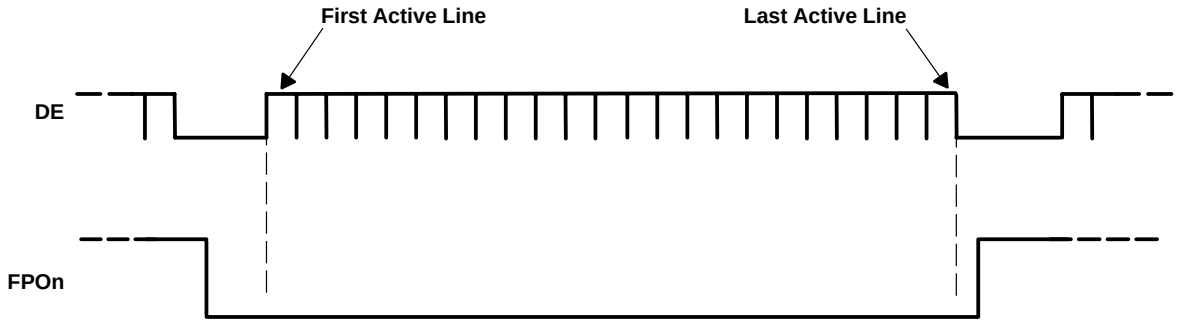


Figure 16. FPOn Programmed With Low Polarity

operation at power on

After powering up, as already described, the device initializes itself, either from the external EEPROM or from the internal ROM. The device then generates one or more frames for initializing the gate drivers and then locks on to the incoming frame structure. While the device is attempting to lock, it remains in auto refresh.

This sequence of events depicted in Figure 17.

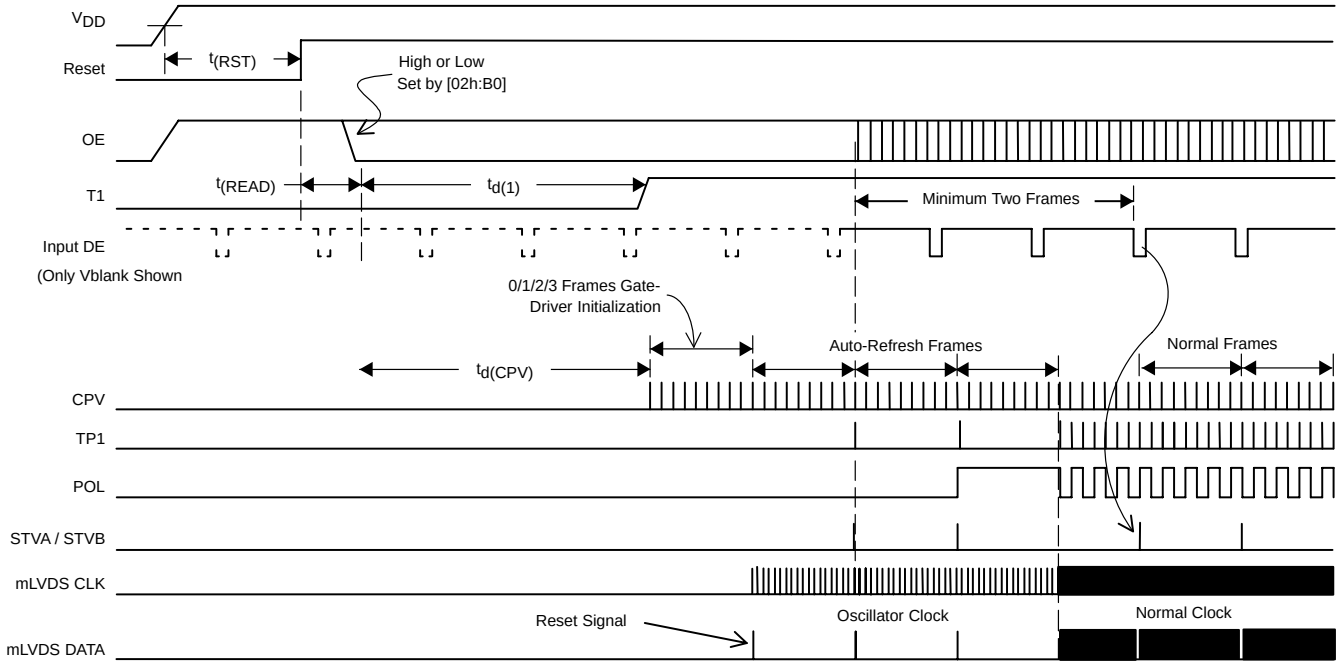


Figure 17. Power-Up Sequence

APPLICATION INFORMATION

auto-refresh operation

The TFP74X3 checks the input signal during operation. If it detects that the input signal is abnormal, it goes into auto-refresh, during which the device operates from the internal oscillator, and writes *all-black* data to the source drivers. Because the internal clock frequency (f_{OSC}) is low compared to the normal operating frequency, the operation during auto-refresh is quite different from normal display operation and the timing signals are generated in a different way. During auto-refresh, TP1 is generated once in a frame. The frame duration is governed by f_{OSC}. The control signals are generated using a separate set of registers, with the resolution of the timing programmability set by t_{OSC} (= 1 / f_{OSC}).

Figure 18 shows what happens when the device enters auto-refresh due to off-spec detection and Figure 19 describes what happens once the input signal is back to normal and the device leaves the auto-refresh mode of operation and comes back to normal operation. Figure 20 describes the auto-refresh operation in detail.

All-black data is all zeros if B5 of register 01h is programmed as 0, and is all ones if it is programmed as 1.

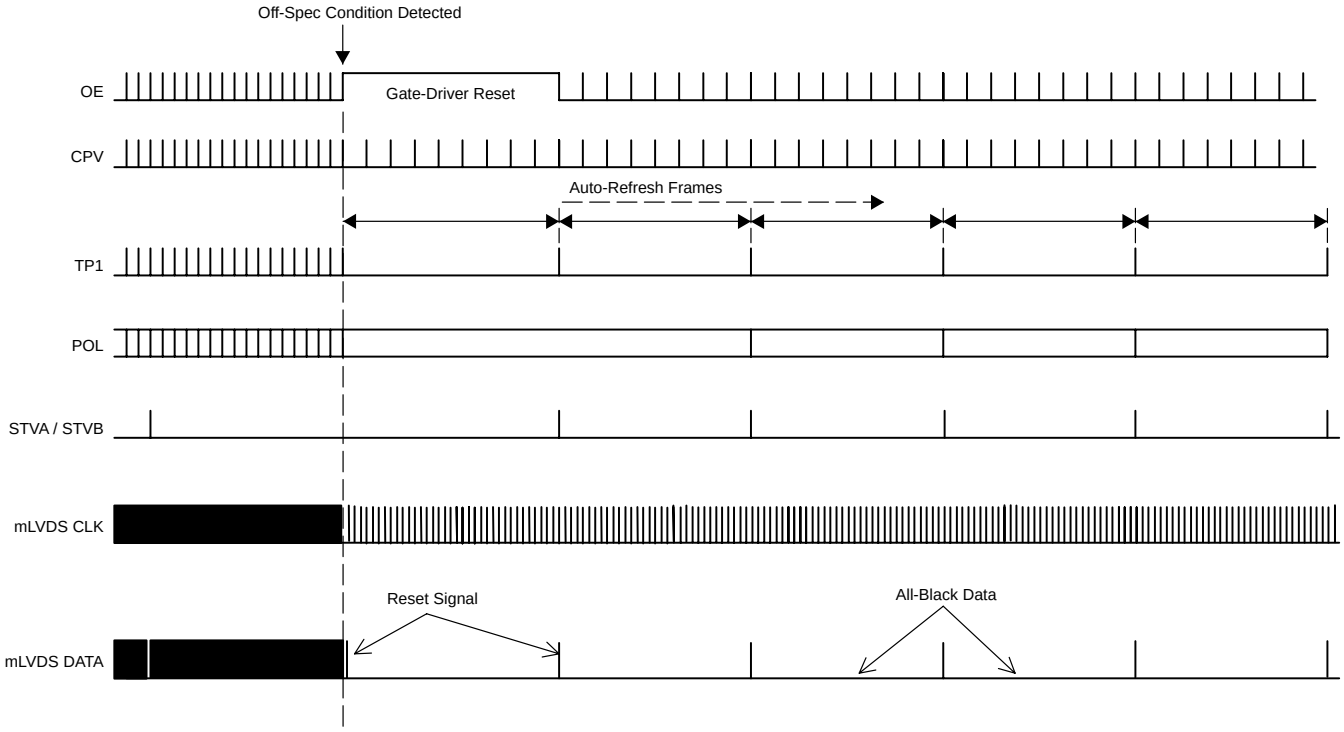


Figure 18. Normal Operation to Auto-Refresh

APPLICATION INFORMATION

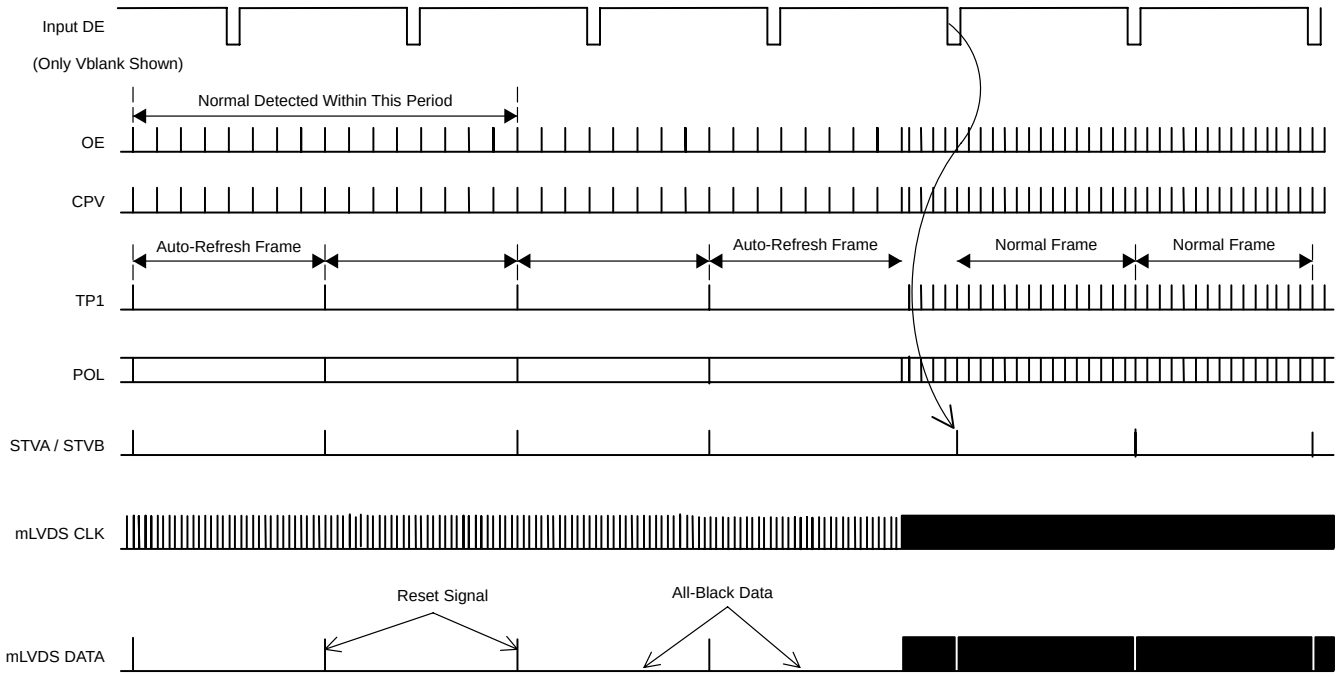


Figure 19. Auto-Refresh to Normal Operation

APPLICATION INFORMATION

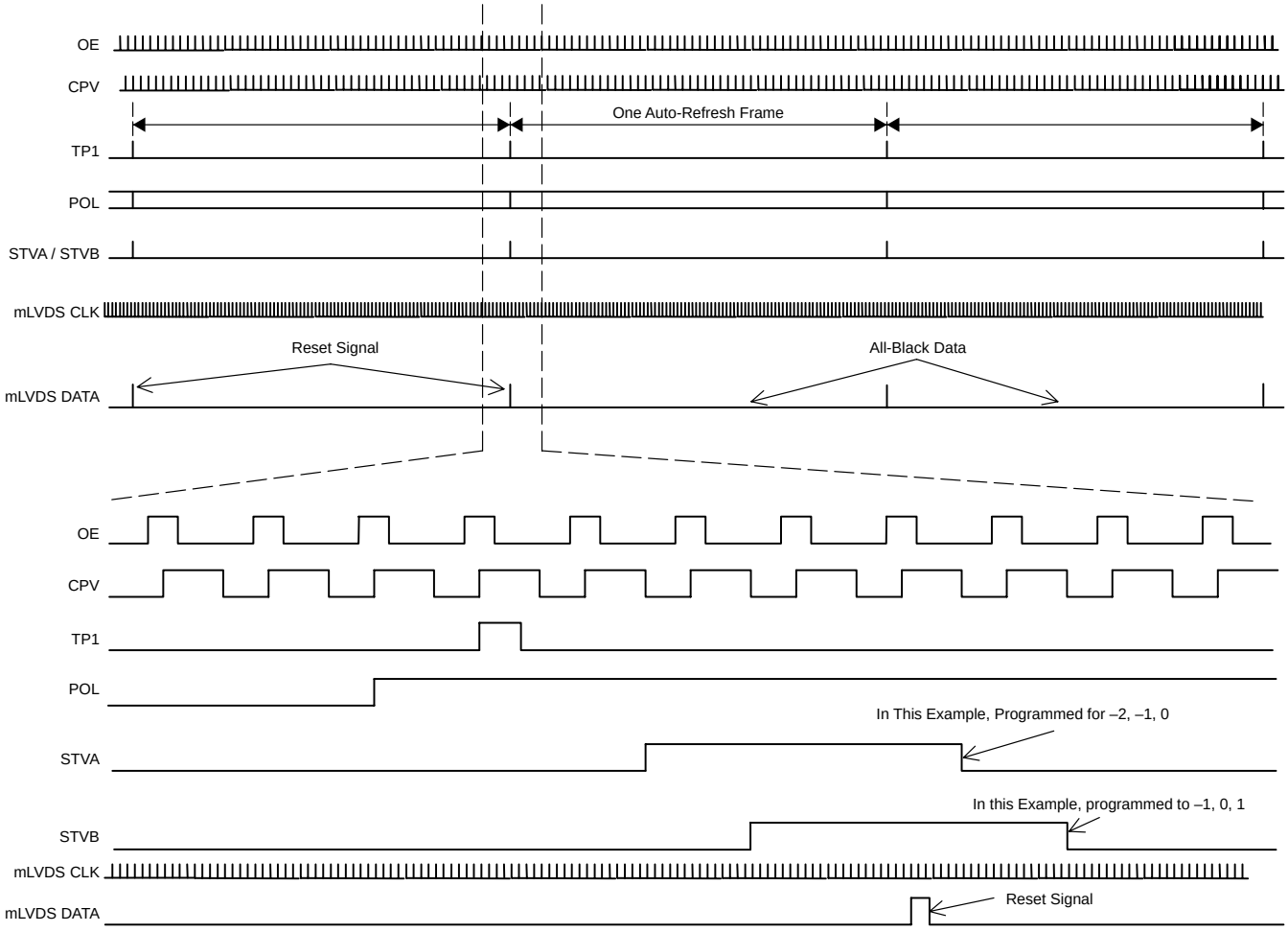


Figure 20. Auto-Refresh Operation Details

aging mode

If the AGING pin is held low during power on, the device enters the aging mode of operation. It needs the FlatLink clock for operation, but otherwise generates patterns internally. The sequence of patterns is shown in Figure 21.

APPLICATION INFORMATION

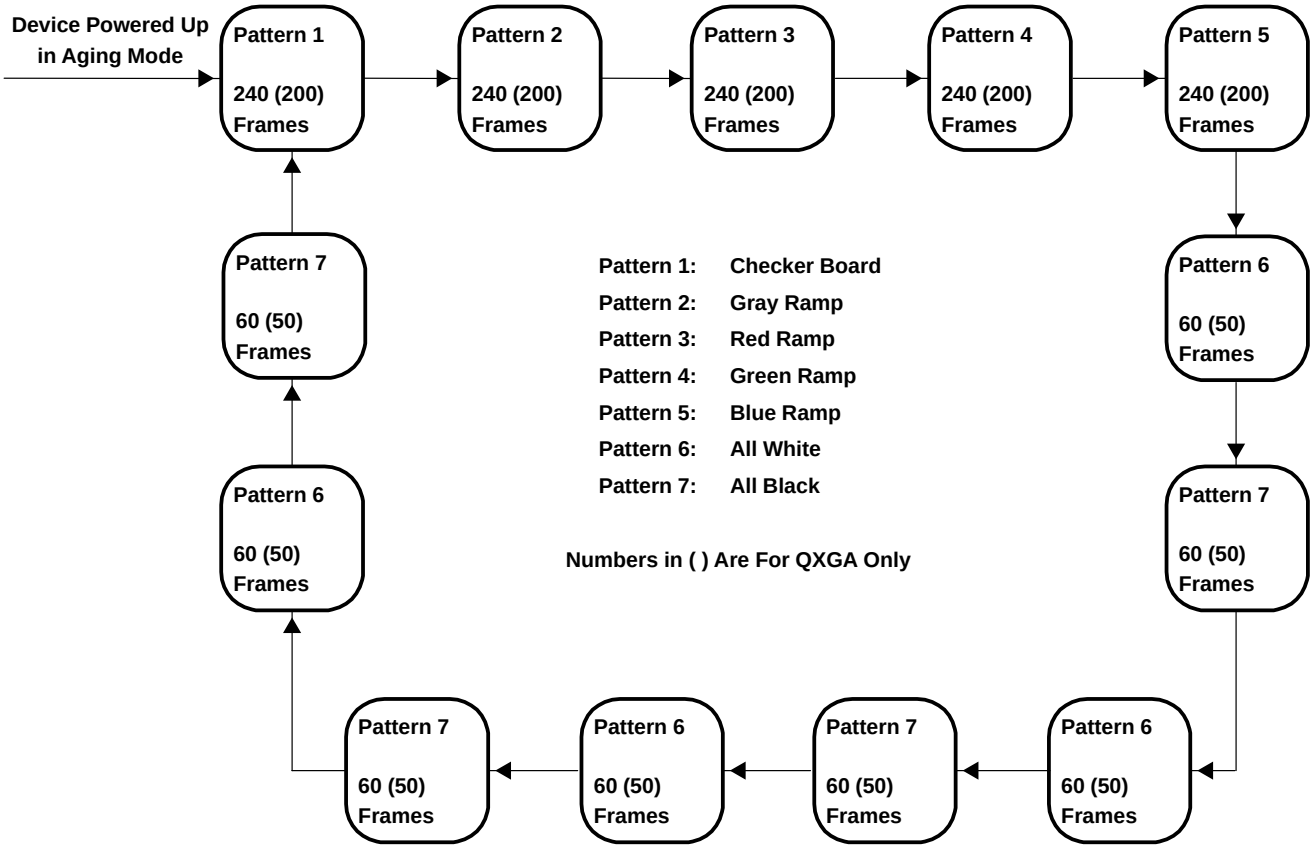


Figure 21. Aging Mode Patterns

normal operation

The way the signals behave during normal operation is shown in Figure 22.

APPLICATION INFORMATION

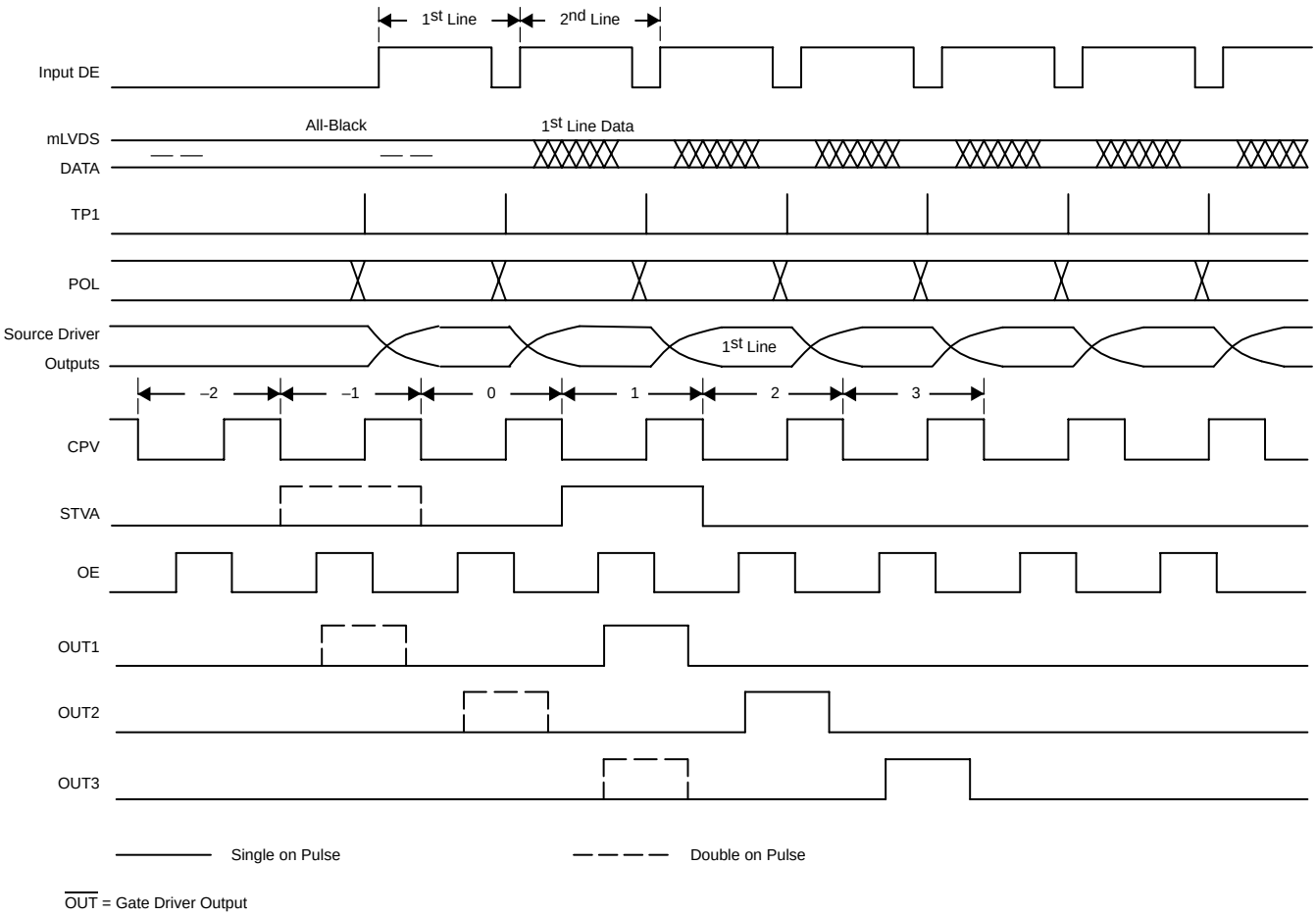


Figure 22. Timing of Normal Operation

typical power consumption

Table 31 shows the typical power consumption for devices of the TFP74X3 family, operating at nominal conditions (room temperature, V_{DD} = 3 V, mini-LVDS current = 3 mA, no pre-emphasis).

Table 31. Typical Power Consumption

DEVICE	RESOLUTION	CURRENT IN DVDD (mA)	CURRENT IN AVDD (mA)	CURRENT IN LVDD (mA)	TOTAL CURRENT (mA)
TFP7423	XGA 60 Hz	29.9	10.5	24	64.4
TFP7433	SXGA+ 60 Hz	56.9	18.5	30	105.4
TFP7443	UXGA 60 Hz	79.3	19.9	36	135.2
TFP7453	QXGA 50 Hz	74.5	19.8	42	136.3

definition of top / bottom mounting

Figure 23 shows a TFT–LCD panel assembly in *un-folded* form with the timing controller top mounted and bottom mounted.

APPLICATION INFORMATION

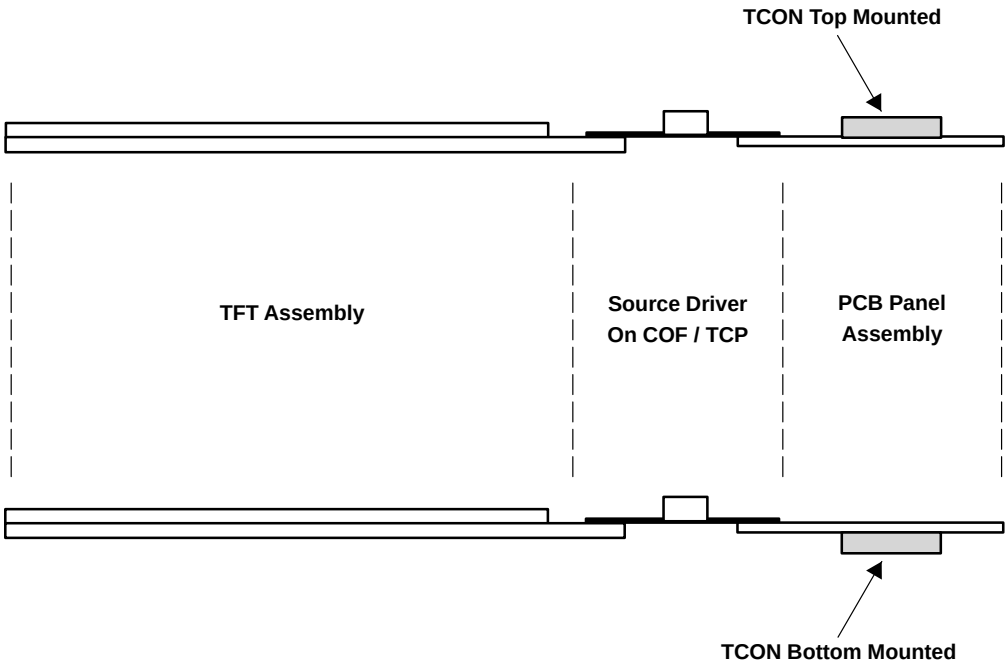


Figure 23. Definition of Top / Bottom Mounting

mini-LVDS PIN ASSIGNMENTS IN DIFFERENT MODES

6-bit and 8-bit XGA

TCON bottom

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
Power down	000R	Power down		000G	Power down	000B
Power down	001R	Power down		001G	Power down	001B
Power down	511R	Power down		511G	Power down	511B

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
		Clock				
512R	Power down		512G	Power down	512B	Power down
513R	Power down		513G	Power down	513B	Power down
1023R	Power down		1023G	Power down	1023B	Power down

TCON top

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
				Clock		
Power down	512B	Power down	512G		Power down	512R
Power down	513B	Power down	513G		Power down	513R
Power down	1023B	Power down	1023G		Power down	1023R

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
000B	Power down	000G		Power down	000R	Power down
001B	Power down	001G		Power down	001R	Power down
511B	Power down	511G		Power down	511R	Power down

mini-LVDS PIN ASSIGNMENTS IN DIFFERENT MODES

6-bit SXGA

PCB top, TCON bottom

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
000R	000G	Power down		000B	001R	001G
001B	002R	Power down		002G	002B	003R
638G	638B	Power down		639R	639G	639B

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
640R	640G	Power down		640B	641R	641G
641B	642R	Power down		642G	642B	643R
1278G	1278B	Power down		1279R	1279G	1279B

PCB top, TCON top

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
641G	641R	640B		Power down	640G	640R
643R	642B	642G		Power down	642R	641B
1279B	1279G	1279R		Power down	1278B	1278G

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
001G	001R	000B		Power down	000G	000R
003R	002B	002G		Power down	002R	001B
639B	639G	639R		Power down	638B	638G

mini-LVDS PIN ASSIGNMENTS IN DIFFERENT MODES

8-bit SXGA

PCB top, TCON bottom

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
000R	000G	000B		001R	001G	001B
002R	002R	002B		003R	003G	003B
638R	638G	638B		639R	639G	639B

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
640R	640G	640B		641R	641G	641G
642R	642G	642B		643R	643G	643G
1278R	1278G	1278B		1279R	1279G	1279B

PCB top, TCON top

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
641B	641G	641R		640B	640G	640R
643B	643G	643R		642B	642G	642R
1279B	1279G	1279R		1278B	1278G	1278R

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
001B	001G	001R		000B	000G	000R
003B	003G	003R		002B	002G	002R
639B	639G	639R		638B	638G	638R

mini-LVDS PIN ASSIGNMENTS IN DIFFERENT MODES

6-bit and 8-bit SXGA+

PCB top, TCON bottom

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
000R	000G	Power down		Power down	000B	001R
001G	001B	Power down		Power down	002R	002G
698B	699R	Power down		Power down	699G	699B

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
700R	700G	Power down		Power down	700B	701R
701G	701B	Power down		Power down	702R	702G
1398B	1399R	Power down		Power down	1399G	1399B

PCB top, TCON top

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
701R	700B	Power down		Power down	700G	700R
702G	702R	Power down		Power down	701B	701G
1399B	1399G	Power down		Power down	1399R	1398B

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
001R	000B	Power down		Power down	000G	000R
002G	002R	Power down		Power down	001B	001G
699B	699G	Power down		Power down	699R	698B

mini-LVDS PIN ASSIGNMENTS IN DIFFERENT MODES

6-bit UXGA

PCB top, TCON bottom

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
000R	000G	Power down		000B	001R	001G
001B	002R	Power down		002G	002B	003R
798B	798B	Power down		799R	799G	799B

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
800R	800G	Power down		800B	801R	801G
801B	802R	Power down		802G	802B	803R
1598G	1598B	Power down		1599R	1599G	1599B

PCB top, TCON top

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
801G	801R	800B		Power down	800G	800R
803R	802B	802G		Power down	802R	801B
1599B	1599G	1599R		Power down	1598B	1598G

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
001G	001R	000B		Power down	000G	000R
003R	002B	002G		Power down	002R	001B
799B	799G	799R		Power down	798B	798G

mini-LVDS PIN ASSIGNMENTS IN DIFFERENT MODES

8-bit UXGA

PCB top, TCON bottom

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
000R	000G	000B		001R	001G	001B
002R	002G	002B		003R	003G	003B
798R	798G	798B		799R	799G	799B

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
800R	800G	800B		801R	801G	801B
802R	802G	802B		803R	803G	803B
1598R	1598G	1598B		1599R	1599G	1599B

PCB top, TCON top

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
801B	801G	801R		800B	800G	800R
803B	803G	803R		802B	802G	802R
1599B	1599G	1599R		1598B	1598G	1598R

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
001B	001G	001R		000B	000G	000R
003B	003G	003R		002B	002G	002R
799B	799G	799R		798B	798G	798R

mini-LVDS PIN ASSIGNMENTS IN DIFFERENT MODES

6-bit and 8-bit QXGA

PCB top, TCON bottom

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
000R	000G	000B		001R	001G	001B
002R	002G	002B		003R	003G	003B
1022R	1022G	1022B		1023R	1023G	1023B

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
1024R	1024G	1024B		1025R	1025G	1025B
1026R	1026G	1026B		1027R	1027G	1027B
2046R	2046G	2046B		2047R	2047G	2047B

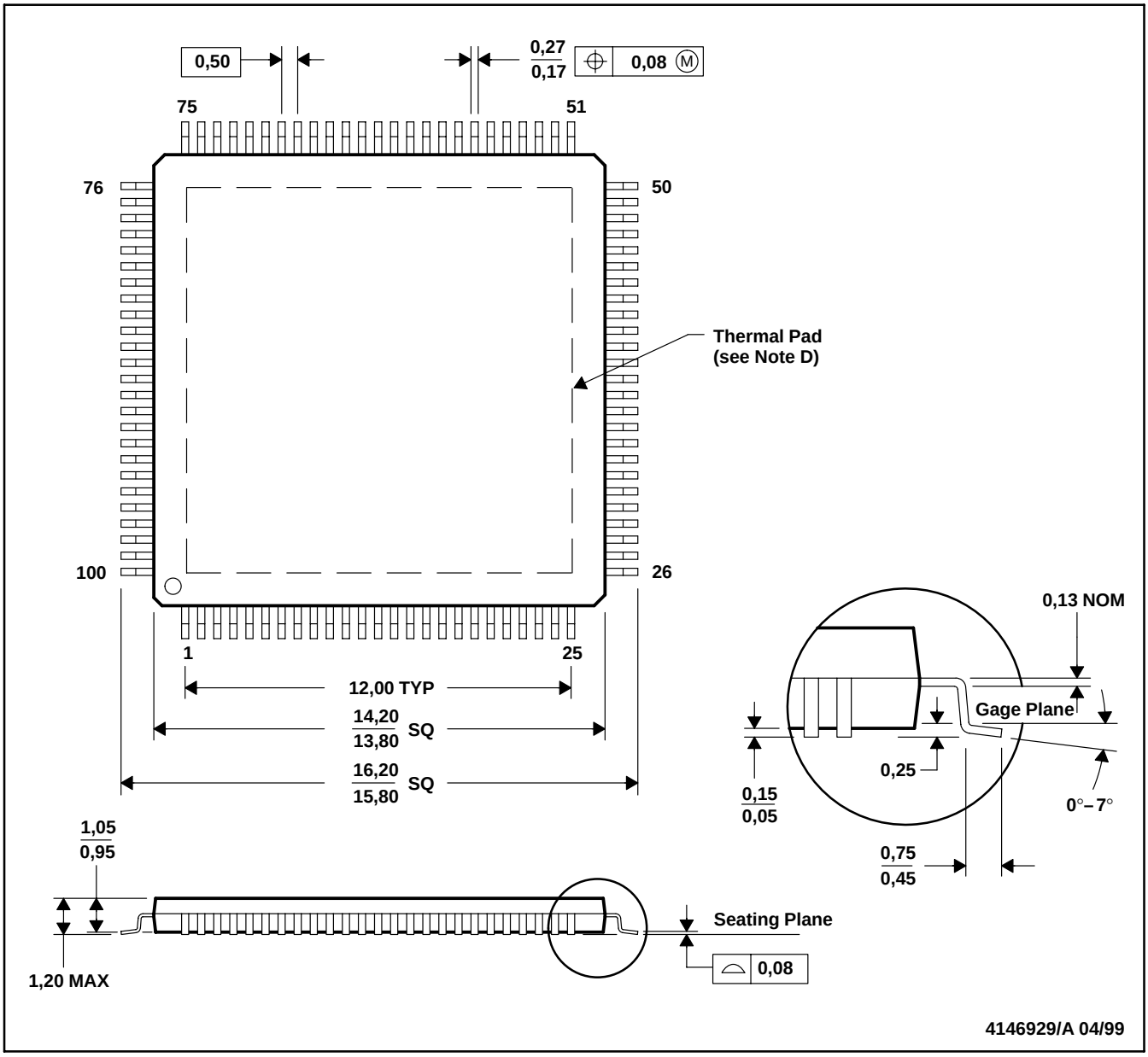
PCB top, TCON top

RLV0	RLV1	RLV2	RLV3	RLV4	RLV5	RLV6
			Clock			
1025B	1025G	1025R		1024B	1024G	1024R
1027B	1027G	1027R		1026B	1026G	1026R
2047B	2047G	2047R		2046B	2046G	2046R

LLV0	LLV1	LLV2	LLV3	LLV4	LLV5	LLV6
			Clock			
001B	001G	001R		000B	000G	000R
003B	003G	003R		002B	002G	002R
1023B	1023G	1023R		1022B	1022G	1022R

MECHANICAL DATA

PZP (S-PQFP-G100) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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