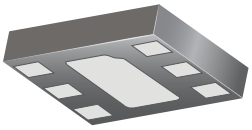
Micropower Ultrasensitive Hall-Effect Switch

Features and Benefits

- 1.65 to 3.5 V battery operation
- Low supply current
- High sensitivity, B_{OP} typically 30 G (3.0 mT)
- Operation with either north or south pole
- Configurable unipolar or omnipolar magnetic sensing
- Complementary, push-pull outputs
- Chopper stabilized
  - Superior temperature stability
  - Extremely low switchpoint drift
  - Insensitive to physical stress
- Solid state reliability
- Small size

Package: 6-pin DFN/MLP (suffix EW)



Not to scale

Description

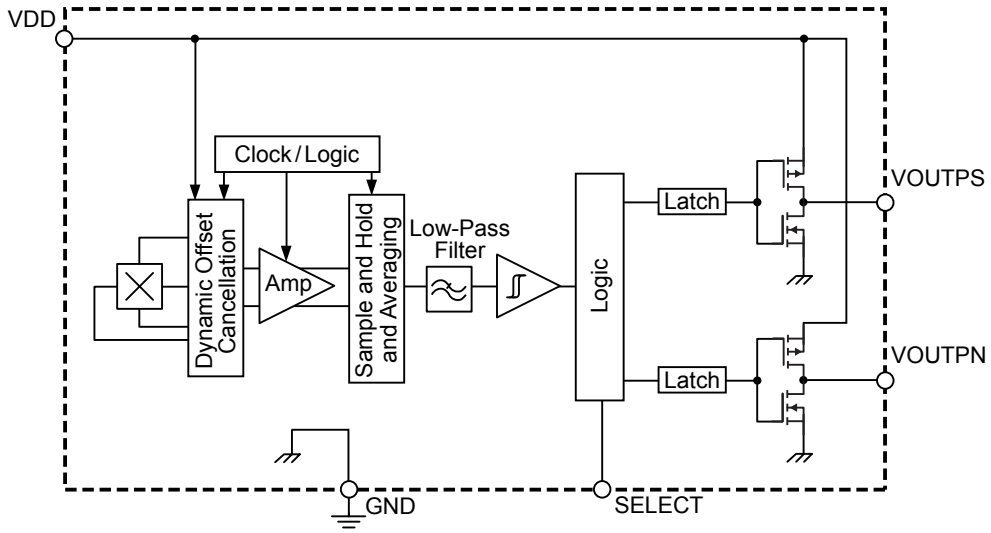
The A1171 integrated circuit is an ultrasensitive, Hall-effect switch with latched digital outputs and either unipolar or omnipolar magnetic actuation. It features operation at low supply currents and voltages, making it ideal for battery-operated electronics. The low operating supply voltage, 1.65 to 3.5 V, and unique clocking algorithm assist in reducing the average operating power consumption. For example, the power requirement is less than 15 μW with a 2.75 V supply.

Unlike more traditional Hall-effect switches, the A1171 allows the user to configure how the device is magnetically actuated. Under default conditions the device activates output switching with either a north or south polarity magnetic field of sufficient strength. The magnetic actuation can be set via an external selection pin to operate in a unipolar mode, switching only on a north or south polarity but not both. Furthermore, the output of the A1171 can be configured to switch either off or on in the absence of any significant magnetic field. Lastly, the A1171 has two push-pull output structures.

This polarity-independence, as well as the minimal power requirements, allows the A1171 to easily replace reed switches,

Continued on the next page…

Functional Block Diagram



Description (continued)

providing superior reliability and ease of manufacturing while eliminating the requirement for signal conditioning.

Improved stability is made possible through dynamic offset cancellation using chopper stabilization, which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress. This device includes, on a single silicon chip, a Hall-voltage generator, a small-signal amplifier, chopper stabilization, a latch, and a MOSFET output.

The A1171 device offers a magnetically optimized solution, suitable for most applications. Package type EW (0.40 mm maximum height) offers a leadless surface mount solution. It is lead (Pb) free, with NiPdAu leadframe plating.

Selection Guide

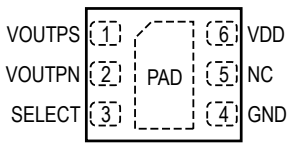
Part Number	Package	Packing[1]
A1171EEWLT-P[2]	DFN/MLP 1.5×2 mm; 0.40 mm maximum height	3000 pieces per 7 inch reel

[1]Contact Allegro™ for additional packing options.
[2]Allegro products sold in DFN package types are not intended for automotive applications.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{DD}		5	V
Reverse Supply Voltage	V_{RDD}		–0.3	V
Magnetic Flux Density	B		Unlimited	G
Output Off Voltage	V_{OUTPx}		5	V
Reverse Output Voltage	V_{ROUTPx}		–0.3	V
Output Current	$I_{OUTPx(Source)}$		1	mA
	$I_{OUTPx(Sink)}$		–1	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Pin-out Diagram



Terminal List Table

Name	Number	Function
VOUTPS	1	Push-pull output (selectable omnipolar activation or unipolar south pole activation)
VOUTPN	2	Push-pull output (selectable inverted omnipolar activation or unipolar north pole activation)
SELECT	3	Sets activation mode for VOUTPx outputs; omnipolar output when tied to VDD or floating, unipolar output when grounded
GND	4	Ground
NC	5	No connection
VDD	6	Connects power supply to chip
PAD	–	Exposed pad for enhanced thermal dissipation

ELECTRICAL CHARACTERISTICS valid over operating voltage and temperature range (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
Supply Voltage Range[2]	V_{DD}	Operating, T_A= 25°C	1.65	–	3.5	V
		Operating, over full ambient temperature range	1.8			
Output Voltage	$V_{OUT(SAT)}$	NMOS on, I_{SINK} = 1 mA, V_{DD} = 2.75 V	–	100	300	mV
	$V_{OUT(HIGH)}$	PMOS on, I_{SOURCE} = –1 mA, V_{DD} = 2.75 V	V_{DD}–300	V_{DD}–100	–	mV
Period	t_{PERIOD}		–	50	100	ms
Chopping Frequency	f_C		–	200	–	kHz
Supply Slew Rate[3]	SR		20	–	–	V/ms
Supply Current	$I_{DD(EN)}$	Device in awake mode (enabled)	–	–	2.0	mA
	$I_{DD(DIS)}$	Device in sleep mode (disabled)	–	–	8.0	µA
	$I_{DD(AV)}$	V_{DD} = 1.8 V, T_A = 25°C	–	3.5	8	µA
		V_{DD} = 3.5 V, T_A = 25°C	–	7.1	12	µA
SELECT Current[4]	I_{SELECT}		0	1	2	µA
SELECT Voltage[4]	$V_{SELECT(LOW)}$		0	–	$^1/_3V_{DD}$	V
	$V_{SELECT(HIGH)}$		$^2/_3V_{DD}$	–	V_{DD}	V

[1]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as T_A = 25°C. Performance may vary for individual units, within the specified maximum and minimum limits.
[2]Operate points, B_{OPX}, and release points, B_{RPX}, vary with supply voltage.
[3]If SR < SR(min), then valid device output might be delayed for one Period, t_{PERIOD}, of device.
[4]Maximum V_{DD}, minimum 0 V.

MAGNETIC CHARACTERISTICS valid at 1.8 V ≤ V_{DD} ≤ 3.5 V and T_A = 25°C

Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units[2]
Operate Point[3]	B_{OPS}		–	32	55	G
	B_{OPN}		–55	–32	–	G
Release Point[3]	B_{RPS}		6	26	–	G
	B_{RPN}		–	–26	–6	G
Hysteresis	B_{HYS}	$\lvert B_{OPX} - B_{RPX} \rvert$	–	6	–	G

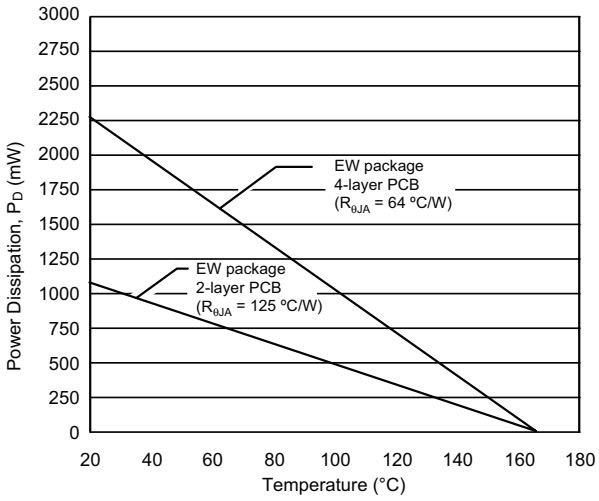
[1]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as T_A = 25°C. Performance may vary for individual units, within the specified maximum and minimum limits.
[2]1 gauss (G) is exactly equal to 0.1 millitesla (mT).
[3]Operate points, B_{OPX}, and release points, B_{RPX}, vary with supply voltage.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

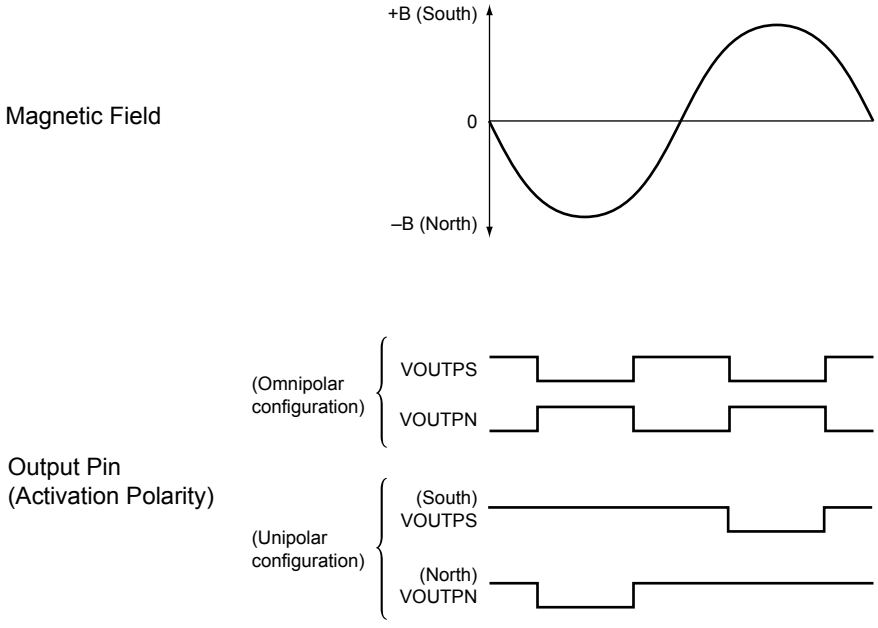
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	2-layer PCB, with 0.23 in.^{2} copper area each side	125	ºC/W
		4-layer PCB, based on JEDEC standard	64	ºC/W

*Additional thermal information available on Allegro Web site.

Power Dissipation versus Ambient Temperature



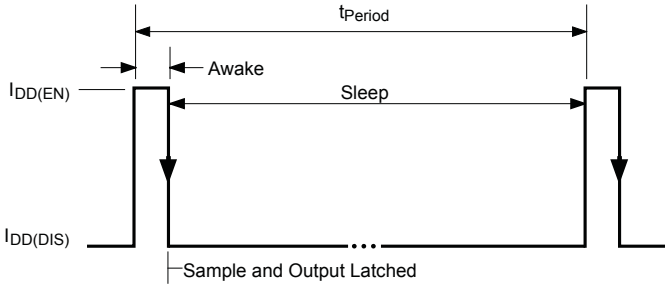
Output Polarity Diagram



Functional Description

Low Average Power

Internal timing circuitry activates the IC for a short period of time, t_{Awake}, and deactivates it for the remainder of the period (t_{Period}). A short awake state duration allows stabilization prior to the sampling and data-latching on the falling edge of the timing pulse. The output during the sleep state is latched in the last sampled state. The supply current is not affected by the output state.



Operation

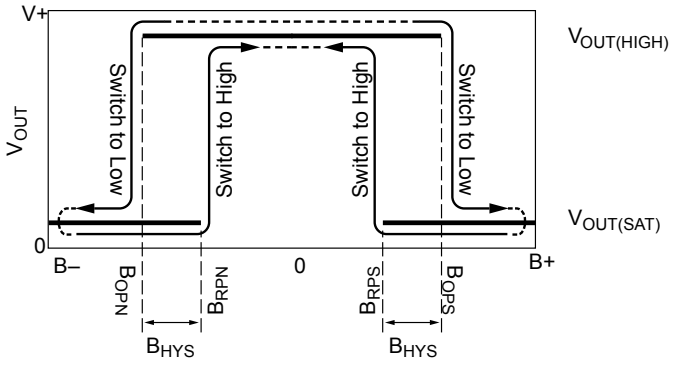
The VOUTPS output switches low (turns on) when the magnetic field received at the Hall element in the A1171 exceeds the operate point, B_{OPS} (or is less than B_{OPN}). After turn-on, the output voltage is $V_{OUT(SAT)}$. The output transistor is capable of sinking current up to the short circuit current limit, I_{OM}. When the magnetic field is reduced below the release point, B_{RPS} (or increased above B_{RPN}), the device output switches high (turns off). The pull-up transistor brings the output voltage to $V_{OUT(HIGH)}$.

VOUTPN operates with the opposite output polarity. That is, the output is low (on) in the absence of a magnetic field. The output goes high (turns off) when sufficient field, or either north or south polarity, is presented to the device.

The difference between the magnetic operate and release points is the hysteresis, B_{HYS}, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Powering-on the device in a hysteresis region, between B_{OPX} and B_{RPX}, allows an indeterminate output state. The correct state is attained after the first excursion beyond B_{OPX} or B_{RPX}.

(A) VOUTPS



(B) VOUTPN

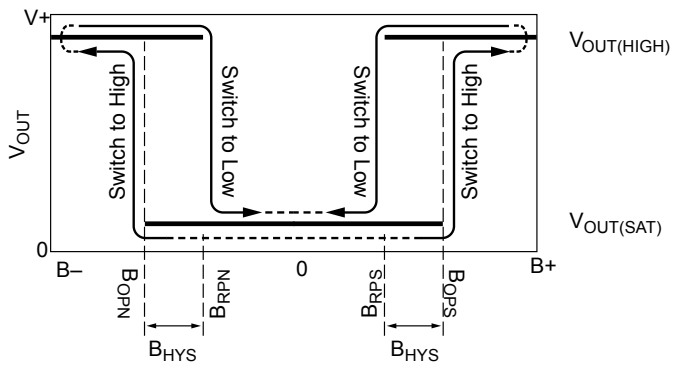


Figure 1. Switching Behavior of Omnipolar Switches. On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity). This output switching profile applies when the SELECT line is allowed to float, selecting omnipolar operation.

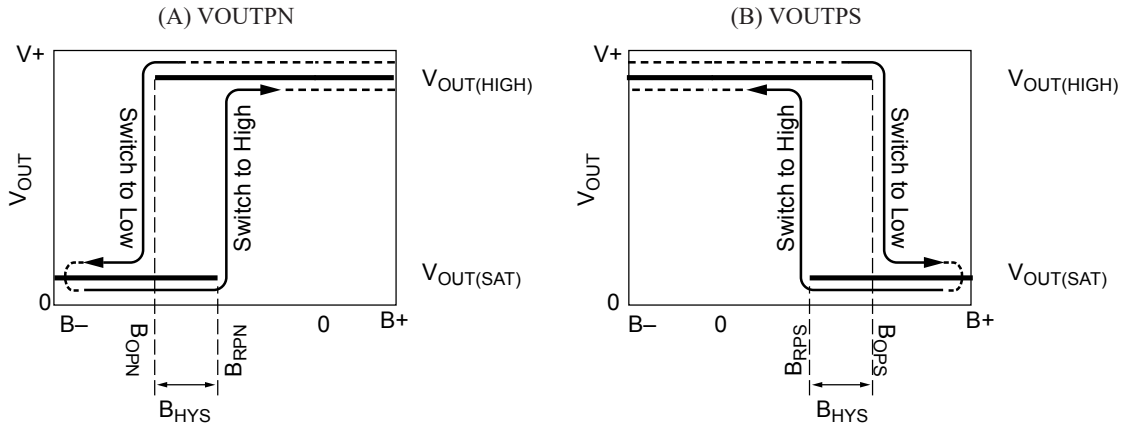


Figure 2. Operation with Unipolar Mode Selected (SELECT Pin Grounded)

SELECT Pin Settings Effect on Output

Output Pin		SELECT Pin Configuration	Output Description
Number	Name		
1	VOUTPS	Tied to VDD or floating	Omnipolar output; ON with magnetic field of sufficient strength ($B < B_{OPN}$ or $B > B_{OPS}$); OFF with low-strength or no magnetic field ($B_{RPN} < B < B_{RPS}$)
		Tied to ground	Unipolar output; ON with south polarity magnetic field of sufficient strength ($B > B_{OPS}$)
2	VOUTPN	Tied to VDD or floating	Omnipolar output; OFF with magnetic field of sufficient strength ($B < B_{OPN}$ or $B > B_{OPS}$); ON with low-strength or no magnetic field ($B_{RPN} < B < B_{RPS}$)
		Tied to ground	Unipolar output; ON with north polarity magnetic field of sufficient strength ($B < B_{OPN}$)

Applications

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization technique. As is shown in figure 3, a 0.1 µF capacitor is typical.

Extensive applications information on magnets and Hall-effect devices is available in the following notes:

- Hall-Effect IC Applications Guide, AN27701
- Hall-Effect Devices: Gluing, Potting, Encapsulating, Lead Welding and Lead Forming AN27703.1
- Soldering Methods for Allegro Products (SMD and Through-Hole), AN26009

All are provided on the Allegro website, www.allegromicro.com.

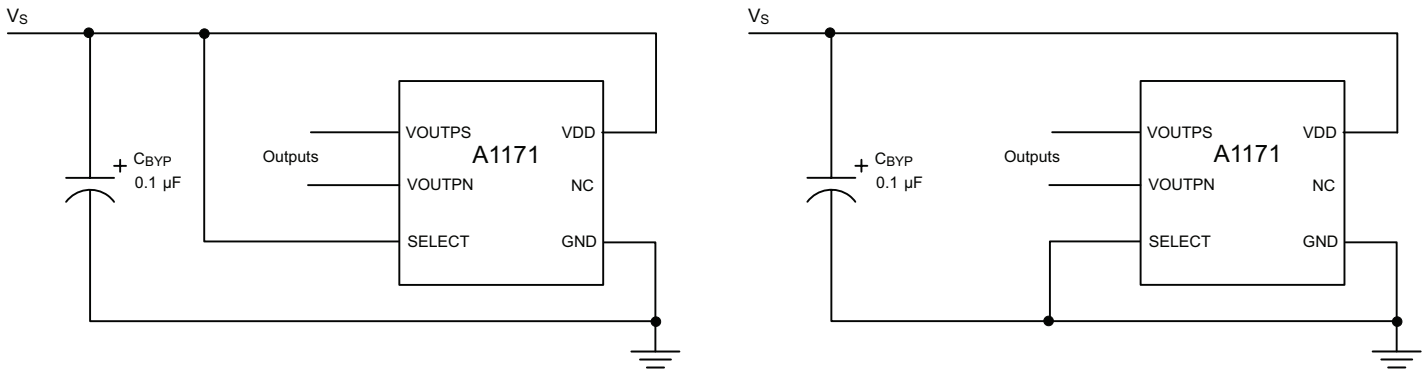


Figure 3. Typical Application Circuits: (a) Omnipolar operation, and (b) Unipolar Operation

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall element. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses.

This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field induced signal to recover its original spectrum at baseband, while the dc offset becomes a high-frequency signal. The magnetic sourced signal then can pass through a low-pass filter, while the modulated dc offset is suppressed. This configuration is illustrated in figure 4.

The chopper stabilization technique uses a high frequency clock. For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling.

The repeatability of magnetic field-induced switching is affected slightly by a chopper technique. However, the Allegro high frequency chopping approach minimizes the affect of jitter and makes it imperceptible in most applications. Applications that are more likely to be sensitive to such degradation are those requiring precise sensing of alternating magnetic fields; for example, speed sensing of ring-magnet targets. For such applications, Allegro recommends its digital device families with lower sensitivity to jitter. For more information on those devices, contact your Allegro sales representative.

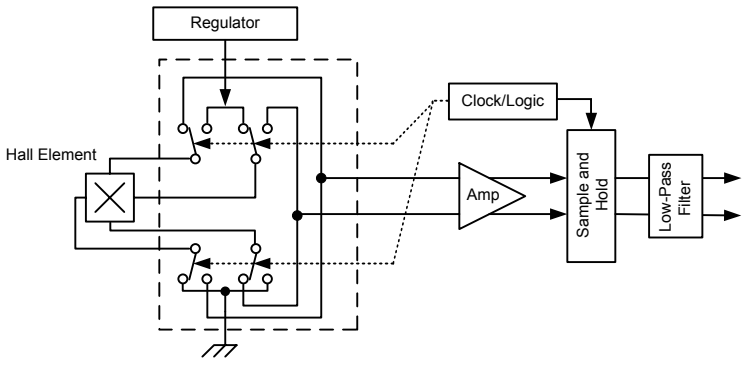
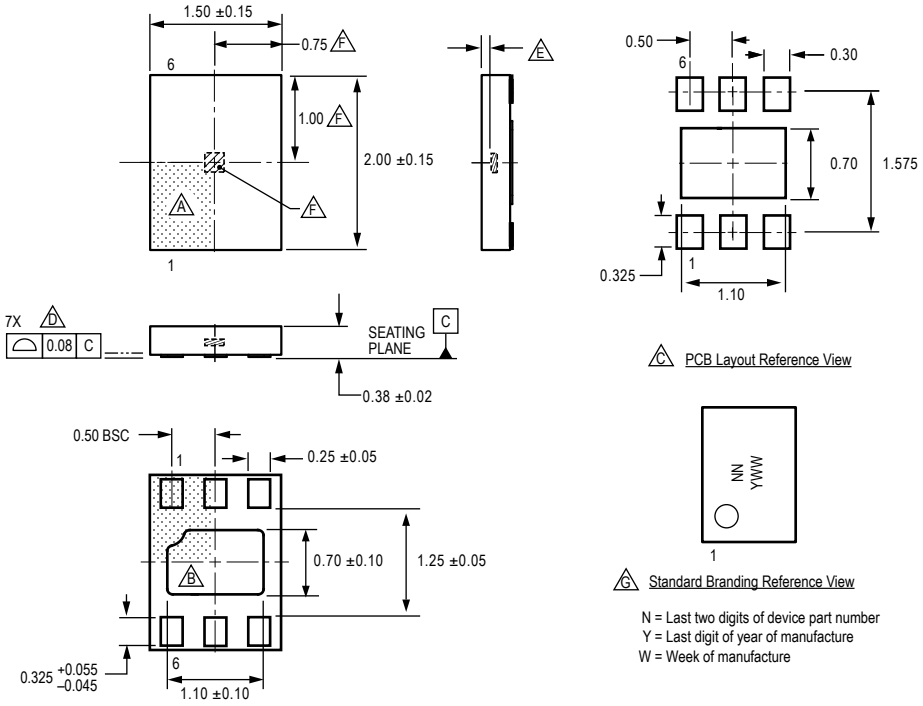


Figure 4. Chopper Stabilization Circuit (Dynamic Quadrature Offset Cancellation)

Package EW, 6-pin DFN/MLP



C PCB Layout Reference View

G Standard Branding Reference View

N = Last two digits of device part number
Y = Last digit of year of manufacture
W = Week of manufacture

For Reference Only, not for tooling use (refernce DWG-2856; similar to JEDEC Type 1, MO-229X2BCD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P200X200X100-9M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Active Area Depth 0.15 mm REF

F Hall Element (not to scale)

G Branding scale and appearance at supplier discretion

Revision History

Revision	Revision Date	Description of Revision
Rev. 5	October 26, 2011	Update Selection Guide
Rev. 6	February 4, 2019	Minor editorial updates

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